The primary author's name was omitted from the following Repository item when it first appeared in September...

R75-241—Bondi, James O. and P. D. Stigall, "Designing and Supporting HMO, an Integrated Hardware Microcode Optimizer" (72 pp., University of Missouri, Rolla, Missouri)

This paper discusses an algorithm for optimizing the density and parallelism of microcoded routines in microprogrammable machines. Besides presenting the algorithm itself, this research also analyzes the algorithm's uses, design integration problems, architectural requirements, and adaptability to conventional machine characteristics. Even though the paper proposes a hardware implementation of the algorithm, the algorithm is viewed as an integral part of the entire microcode generation and usage process, from initial high-level input into a software microcode compiler down to machine-level execution of the resultant microcode on the host machine. It is believed that, by removing much of the traditionally time-consuming and machine-dependent microcode optimization from the software portion of this process, the algorithm can improve the overall process.

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R75-283—Barquin, Ramon C., "A Survey of Computer Education in Latin America" (31 pp., IBM A/FE Corporation, MIT, Cambridge, Massachusetts)

The article reviews the existing computer education programs throughout the region. Although the principal focus is on programs at the university level, education being given by other sources is also covered. Among these, of course, are the offices of the manufacturers, private data processing schools, government trade institutes, high schools, etc. A classification of the university programs is attempted based on the existence of given courses, concentrations, basic degree programs, or post-graduate degrees. The main sources for this information are 1) personal visits and interviews by the author on a six-month MIT sponsored field research on computation in Latin America and 2) the "Boletin Ibero-americano de Centros Universitarios de Computacion." Several analyses attempting to relate, or correlate, the state of computation and level of computer-user sophistication to the quality and quantity of the relevant education are included. These are done within the context of the different countries' general educational statistics. In addition, the partial results of a survey conducted during the past two years which attempts to obtain a profile of the Latin American computer professional are provided. Based on these results and the general information gathered by the author during his field research, some guidelines are offered concerning future trends that should benefit computer education in Latin America.

R75-284—Maryanski, Fred J. and Taylor L. Booth, "Inference of Finite-State Probabilistic Grammars" (47 pp., Kansas State University, Manhattan, Kansas)

The problem of inference of finite-state probabilistic grammars is studied from two points of view. First, the theoretical aspects of grammatical inference are considered. Among the topics investigated are the structural and statistical properties of
probabilistic grammars, methods for assigning probability measures to rewrite rules of probabilistic grammars, and statistical measures for determining how well an inferred probabilistic grammar approximates a sample set. The second concern of the study is the development of a sample set within a user-supplied acceptance region under the chi-square test. This procedure is enumerative with tree-searching techniques used to improve efficiency. The convergence of the procedure with an acceptable grammar is demonstrated, and the steps of the procedure are theoretically justified. Test results are presented. The inference procedure developed provides a means of synthesizing a probabilistic model of both physical and abstract systems from samples of their behavior.

R75-285—Unger, Stephen H., "The Generation of Completion Signals in Iterative Combinational Circuits" (16 pp., Institutet for Datateknik, Lyngby, Denmark)

It is shown that if a flow table has synchronizing sequences they can be used, at little added cost, to reduce substantially the average delay in combinational iterative realizations that generate completion signals. This constitutes a generalization of earlier work by Waite. Some quantitative results are presented indicating the extent of speed-up to be expected.

R75-286—Brakefield, James, "Aspects of Computer Architecture" (20 pp., Technology Inc., Life Sciences Division, San Antonio, Texas)

In the context of medium and large computer architecture, hardware design options are presented which allow software algorithms to remain invariant over a range of computer word sizes. Use of descriptors for referring to memory plays an integral role. The paper is taken of choosing a specific data format for floating point numbers. Advantage is taken of the arithmetic characteristics of the commonly used word sizes. A variety of other hardware and software design possibilities are mentioned.

R75-287—Yuen, C. K., "On the Walsh Transform of a Shifted Vector" (20 pp., Australian National University, Canberra, Australia)

The relation between the Walsh transforms of a vector before and after a shift operation is studied. The two transforms are related by a matrix multiplication. A fast algorithm requiring 2n/2 additions and 2n/2 development and implementation of this matrix multiplication is presented.

R75-288—Petzold, R. L., Richter, H.-P., Rohrs, "A Two Level Microprogram Simulator" (7 pp., Universität Dortmund, Germany)

This paper reports our current progress at the Department of Informatik of the University at Dortmund in investigating problems of dynamic microprogramming. In order to get a suitable tool quickly we decided to develop a corresponding simulator. The design criteria of a simulator for a two level QM-1-like microstructure are briefly described. Of primary interest are the methods for the serialization of time parallel events. Two different procedures are described. By means of the features of the used simulation language APL SV it was possible to achieve as well a flexible and easily extendable microprogramming structure as a convenient accessible model for problems of dynamic microprogramming. An example of a microprogrammed complete priority interrupt handling feature is appended.

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R75-289—Erich, Roger W., "Representation of Random Waveforms by Relational Trees" (34 pp., University of Massachusetts, Amherst, Massachusetts)

In a number of applications of image processing, much information about objects or textures in the image can be obtained by sequential analysis of individual scan lines. In this paper a method is proposed for representing a random waveform by a relational tree that provides a two-dimensional description of the structure of the waveform. Unlike most earlier methods that were grammatical in nature, this algorithm is object independent, and it is deterministic, and fast. The relational tree is a versatile data structure that facilitates the extraction of information for specific one and two-dimensional processing tasks. The intended applications include robotics and texture analysis, and several such applications are explored.

R75-290—Cheung, Lawrence S. and Frederic J. Mowle, "Suggestions for Improving the Effectiveness of a Parallel Computer System" (45 pp., Marquette University, Milwaukee, Wisconsin, and Purdue University, West Lafayette, Indiana)

The effectiveness of a parallel single processor computer system is limited by the dependencies among its instructions. The types of dependencies can be classified into three categories: procedural dependency which arises from jump instructions; operational dependency which arises when a resource associated with the operation specified by an instruction is busy; and data dependency which arises in a sequence of instructions when an instruction effects the source operands of any other instructions that come after it. An approach is suggested to cope with some of these problems. This includes the enhancement of a conventional instruction set and the specification of a computer system with jump instruction look ahead capability. An efficient data routing scheme, which can reduce the effect of data dependency, was incorporated into the design of the processor. The effectiveness of these suggestions was evaluated using simulation and significant improvements were obtained. In order to reduce operational dependency at a minimum cost, a model for a shared resource multiprocessor was formulated to study the relationship among hardware utilization, program response time, and system balance. The importance of the limit case when there is an infinite number of programs in the system was also emphasized.

R75-291—Chevance, R. J., "A Machine Architecture for Non-numerical Processing" (25 pp., Compagnie Internationale Pour L'Informatique, Louveciennes, France)

A machine architecture oriented towards the interpretation of user defined data structures and operators is presented. New data types and operators are expressed in terms of more basic ones. The machine is based upon stack structure and descriptors. A data descriptor refers to a program, the addressing program, whose purpose is to interpret both operators and data structure as well as to handle error or special conditions. This approach allows the attachment of error/condition handling routines to any particular object. The formats of descriptors, stacks, instructions, and extended instructions are described.


This paper explains how to use a software reliability estimation program that computes present mean time to failure (MTTF), percentage of MTTF objective attained, remaining number of failures to be uncovered and corrected to achieve the MTTF objective, remaining execution time and calendar time required to reach the objective, and some other quantities. A "most likely" (maximum likelihood) value and 50, 75, 90, and 95% confidence intervals are computed. The predictions are based on intervals between failures experienced during testing of the program.

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This paper provides the program documentation for a software reliability estimation program that computes present mean-time-to-failure (M T F ) and percentage of MTTF objective attained, remaining number of failures to be uncovered and corrected to achieve the reliability objective, remaining execution time and calendar time required to reach the objective, and some other quality data. A "most likely" (maximum likelihood) value and 50, 75, 90, and 95% confidence intervals are computed.


A slotted ALOHA System with non-instantaneous response is analyzed. The throughput, delay, recovery time, and failure time variations are plotted as functions of active and blocked users' starting times. From these curves, delay vs throughput, recovery time vs throughput, and failure time vs throughput curves are obtained. The optimum delay as well as recovery time are shown to be monotonically increasing functions of throughput, whereas failure time is shown to be a monotonically decreasing function of throughput. Control policies to achieve good performances are found. The performance of the system under these policies is tested. Satisfactory performance is achieved in all the quantities with these policies. The results of this system are compared with those of the instantaneous systems. The differences are listed. The significance of these differences is explained in detail.


A slotted ALOHA System without blocking and a finite number of users is modeled. The average throughput, delay, recovery time, and failure time are obtained for the model. A new quantity, the average number of packets discarded is also defined and evaluated. The system behavior with the variation of the number of users is studied in detail. The control procedures to achieve the maximum throughput are given. This system is then compared with a system with blocking. Finally, the effect of blocking is quantified, in terms of channel bandwidth.


A slotted ALOHA with blocking is analyzed. This model assumes instantaneous response from all users. The throughput, delay, average recovery time, and the average failure time variations are studied in detail. Various static control procedures to improve the performance are described and tested for their performance.

R75-297—Murthy, Parimi, “Augmented State Analysis of Slotted ALOHA with Blocking” (18 pp., Technical Report B75-10, University of Hawaii, Honolulu, Hawaii)

A slotted ALOHA System with blocking and instantaneous response is analyzed by a new technique called "the augmented state analysis." The exact delay expression is derived using the properties of finite Markov chains. The numerical values obtained by the new analysis are very close to the values of the previous analysis in the region of interest. Two other parameters, the individual user's recovery time and the time a user spends in the blocked mode, are also defined and analyzed in detail.


This paper describes an algorithm, and a PL/I program (SYM-1) implementing it, that detects symmetry of a variable-valued logic function with regard to the variables or their inverses. If symmetry exists, symmetric variables are then used in symmetric selectors which will describe the set of events in a more compact way than corresponding non-symmetric selectors.


Large scale integration in semiconductors has brought about concepts in devices, circuits, and systems to be blended into the design of LSI devices. Here, the fundamentals of LSI charge coupled devices in regard to their specific usage as computer memories are given. In a manner such that system, circuit, and device designers can get a flavor of all the ramifications of this new device. Charge coupled memory chip and system design tradeoff considerations are explained. The applications of charge coupled memories in computer memory hierarchies and computing systems are suggested.

The paper is divided into two distinct sections: "Charge Coupled Memory Technology" describes the physical operation and the fabrication of charge coupled memory devices; "Charge Coupled Memory Devices and Systems" concentrates on the different organizations of the device and their application to computing systems.

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Not generally available elsewhere, this manual provides complete documentation for SURGE717, a non-proprietary computer program which generates appropriate data-processing logic and produces COBOL source programs from simple descriptive parameter cards.

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A BASIC language interpreter has been designed for use in a microprocessor environment. This report discussed the development of 1) an elaborate text editor and 2) a table driven interpreter. The entire system, including text editor, interpreter, user test buffer, and full floating point arithmetic routines fits in 16K words.

Price, photocopy—$5.20