REPOSITORY

The Repository, a collection of over 2000 technical papers and documents relating to computer science and engineering, is maintained by the Computer Society as a service to the information processing community. Some of the papers have been refereed; others have not.

If you have a paper of interest to the computer field, you are invited to submit two copies to Dr. Warren L. Semon, IEEE Computer Society Editor-in-Chief, Division of Systems and Information Sciences, 313 Link Hall, Syracuse University, Syracuse, NY 13210. Be sure to include a cover letter giving permission to enter the paper in the Repository. Entry in the Repository does not constitute publication.

Photocopy prices are $.10 per page. A $1.00 shipping and handling charge will be added to all orders under 50 pages. Microfiche copies are available at $2.50 for each 50 pages of copy. Minimum incremental charge: $2.50.

Be sure to state the R number, listed before the author's last name, of each paper you order. All Repository items must be prepaid except for companies or institutions with established accounts. A $2.00 invoice charge will be added to all non-prepaid orders. Please make your check or money order payable to the IEEE Computer Society.

R75-213—Mavaddat, F. and B. Parhami, "Two-Level Associative Memory Organization for Table Look-Up Applications" (21 pp., Technical Report No. CSL-74-001, Computer Systems Laboratory, Arya-Mehr University of Technology, Tehran, Iran)

A two-level associative memory organization is a combination of a small associative memory and a conventional memory, which behaves like a large associative memory most of the time when queries from a special class of associative type are posed. In this paper, such an organization is proposed and evaluated through simulation, for table look-up operations of the type encountered in assemblers and compilers. Motivation for this work is the prohibitive cost of large associative memories. Simulation results are consistent with those obtained for cache memories and show that a large percentage of the queries can be answered by the associative memory without a need to reference the conventional memory. The associative memory is specially designed for automatic implementation of the LRU (least recently used) replacement algorithm. The conventional part of the memory may be part of the main store of the system into which the two-level associative memory is incorporated.


Storage allocation methods for arrays, either at compile-time (static) or run-time (dynamic), by the nature of the addressing polynomial, require the size of each dimension (except possibly one) to be fixed at the time the addressing is being performed. An allocation scheme with a corresponding addressing polynomial independent of dimension size for square and n-cube arrays (arrays having equal size in each dimension) has been developed, which allows the array size to vary even as the addressing is being performed. The resulting structure can also be considered as a multidimensional generalization of a stack. Using the notation of \( a, b, \ldots, x \) to represent \( a_1 p_1^n - 1 + a_2 p_2^n - 2 + \ldots + a_0 p_0 ^0 \) and assuming \( a_m \) to be the leftmost maximum among the indices \( (a_1, a_2, \ldots, a_n) \), the polynomial for the n-cube array is derived as \( f(a_1, a_2, \ldots, a_n) = f(0, 0, \ldots, 0) + (a_1 a_2 \ldots a_n a_m + 1 + a_m - a_m - a_m \cdot a_1 a_2 \ldots a_n a_m \) which reduces to \( f(1, 2) = f(0, 0) + a_m + a_1 + (2 - m) \cdot a_2 \) for the two dimensional case.


Character decomposition methods are discussed by which the performance of character output devices can be improved. This increased performance can be manifested both by increase of speed and extension of character space—or a traded-off combination of both. Correspondingly, the functional characteristics of character output devices are discussed which can take advantage of this increased performance. These ideas are applied to the compromised design of Farsi alphabet which with minor modifications are also applicable to Arabic script. This can be useful in design of printing devices used in countries with more than three hundred million people. It is believed that these methods could also be applied to other scripts with the cooperation of the people conversant in those languages.

R75-216—Parhami, B., "Application of APL for Rapid Verification of a Digital System Architecture" (9 pp., Technical Report No. CSL-75-002, Computer Systems Laboratory, Arya-Mehr University of Technology, Tehran, Iran)

An instruction set for a special-purpose associative processor, designed for information storage and retrieval applications, is defined in APL/360. These definitions are then used to test the validity of the system's architecture for the proposed applications. This is accomplished by writing and simulating the execution of sample programs on a sample data set and selectively observing the corresponding transformations performed on the data set.

Order by R-number. Use the Repository order form on page 72.

September 1975
R75-217—Parhami, B., "Errors in Digital Computers: Causes and Cures" (23 pp., Technical Report No. CSL-75-003, Computer Systems Laboratory, Arya-Mehr University of Technology, Tehran, Iran)

Errors in digital computers are caused by two classes of faults: design faults which may exist in hardware or software of the system, and operational faults due to component failures or external interference during system operation. This paper provides an introduction to various causes of errors in digital computers and measures that can be taken to avoid such errors.

R75-218—Parhami, B., "Modeling of Trade-offs in Fault-Tolerant Homogeneous Array Processors" (17 pp., Technical Report No. CSL-75-004, Computer Systems Laboratory, Arya-Mehr University of Technology, Tehran, Iran)

Array processing has been used as a technique to improve the performance of digital computer systems. The problem of reliability for array processors is of major concern since the extreme complexity of these machines makes them highly susceptible to hardware failures. In this paper, a reliability modeling procedure is presented for a class of fault-tolerant, homogeneous array processors with a hard-core configuration switch. The cost/reliability trade-offs implied by the model are discussed and an example is presented for illustration. It is shown that reliability gain is possible by increasing the total system cost, but only to a certain point. However, before reaching this point, many different reliability levels can be attained at varying costs.

R75-219—Mavaddat, F., "An Experiment with Teaching of Programming Languages" (34 pp., Technical Report No. CSL-75-005, Computer Systems Laboratory, Arya-Mehr University of Technology, Tehran, Iran)

After some reflections upon difficulties involved in teaching programming in an introductory course, a simple programmable machine of mechanical nature with a small set of very simple instructions is presented.

All the necessary concepts such as sequencing, looping, subroutines, and declarative statements are introduced in the framework of this machine, and a number of problems are assigned to gain experience in use of such concepts. At closing, it is argued that a simplification of most programming languages is easily teachable by relating them to the concepts developed for this machine. A simplification of Fortran is treated for this purpose.

R75-220—Parhami, B., "Representation of Digits by Optically Weighted Dot-Matrix Characters" (17 pp., Technical Report No. CSL-75-006, Computer Systems Laboratory, Arya-Mehr University of Technology, Tehran, Iran)

Representation of digits by optically weighted characters is a way of representing information in combined digital and analog form. Such characters can be used to represent three-dimensional patterns on conventional printers, with the third dimension visualized by the darkness of various printed page areas. In this paper, a general framework for the design of optically weighted characters to represent digits is established, and several examples are given to illustrate the general concepts. It is shown that Farsi digits lend themselves very well to optically weighted representation, and examples of such character sets are given for both decimal and hexadecimal Farsi digits.

R75-221—Rampapirian, H. K., "Data Handling for the Geometric Correction of Large Images" (31 pp., Computer Sciences Corporation, Huntsville, Alabama)

Several geometric distortions are present in remotely sensed images depending on the type of sensor used to observe the object being observed. It is often desirable to correct for these distortions and store the images in reference to a standard coordinate system. Digital techniques for correction are versatile and introduce a minimum of radiometric errors. The main problems to be considered in this area are the determination of the correct transformation, resampling, and the management of the large quantities of data. This paper considers the last problem. It is shown here that, by a judicious rearrangement of the input data, considerable reductions in the memory capacity can be achieved. The rearrangement can be accomplished in several states. The method presented here is amenable to pipeline implementation for processing a continuous stream of images. It may also be used on a relatively small computer with the staging being in time sequence rather than hardware. Examples are shown to illustrate the reductions in overall cost depending on the relative cost of memory and the peripheral devices.

Order by R-number.
Use the Repository order form on page 72.
The purpose of this report is to describe the ALOHA System's radio communication sub-system at a functional and block diagram level. The material is separated into descriptions of the types of stations used in the system, the data interface between the radio sub-system and the data terminal equipment, the modulation scheme employed, and the radio transceiver and modem equipment. In addition, results of radio range measurements are provided with comparisons to predicted ranges. Also, some results of impulse noise measurements are given, with a discussion about the possible effects on burst data transmission by urban impulse noise.

The major result of this paper is that fixed length packets maximize throughput and minimize delay for an unslotted ALOHA random access channel. The model studied assumed that a terminal sends a packet with arbitrary length and then waits an exponential length time (mean $\lambda^{-1}$) before attempting to transmit again. Each time it transmits, it obtains a new independent message length according to $L(t)$. This model discriminates against long packets by not requiring repeated successive retransmissions in the event of failure. Even with this optimistic view, fixed length packets maximize throughput. The throughput for arbitrary $L(t)$ is computed and specialized for a few examples. This paper represents an extension of a previous paper where $L(t)$ was assumed exponential.

In this paper we provide a survey of the history, technology, and economics of commercial satellite data communications. Technological, economic, and locational trends in satellite data communications are examined, and the differences between the satellite channel and terrestrial channels are emphasized. After a discussion of existing standard tariffed satellite data services, we list some possible tariffed data services, which might be offered to take advantage of the special properties of satellite data channels.

A technique is presented that uses both cluster analysis and a Monte Carlo significance test of clusters to discover associations between variables in multidimensional data. The method is applied to an example of a noisy function in three-dimensional space and also to a sample from a mixture of three bivariate normal distributions.

A simulator has been implemented which produces simulated telemetry data for the high speed image (radiometer) channel and the attitude part of the housekeeping channel. In this paper we describe parts of this simulator which are interesting from the point of view of image and computer graphics. The simulator was implemented on an IBM 370/155 using an IBM 2250 display, a microfilm recorder SD4060, and a photowrite unit—OPTRONICS International.

A high-speed minicomputer with a cache memory, complete I/O, break and interrupt facilities, implementing the entire PDP-8 instruction set has been designed. Complete instruction execution of 125 machine cycles is possible. The design of this machine was greatly facilitated by the use of a fast interactive simulation program with macro and array features. Several output timing formats provided minimum output data of maximum usefulness because of the dependence of the density of the data on its dynamic activity.

IEEE Computer Society Repository
Cumulative Index 1966-1973

Published by request of Repository users, the cumulative index lists just under 1600 entries for 1966 through 1973. It consists of three parts: an author index, a subject index based on keywords, and a chronological index in the order in which the items have been listed through the years.

Price—$16.00 Member Price—$12.00

To order: Use the multipurpose order form on page 71.
R75-237—Kohout, L. and B. R. Gaines, "The Logic of Protection" (24 pp., Dept. of Electrical Engineering Science, University of Essex, United Kingdom)

This paper presents a brief exposition of the role of various mathematical techniques in the development and utilization of resource protection structures for computers. The first section is concerned with the semantics of the problem—the distinction between protection problems in general and those whose complexity necessitates deeper theoretical treatment. The second section considers the roles of algebraic, topological, and modal/multi-valued logical, techniques in the analysis of protection. Finally, we give an analysis of a current protection model to illustrate the problems and techniques.

R75-238—Tse, B. K. P., "Caeotron: A Tube for the Blind" (83 pp., Technical Report UIUCDCS-R-75-705, Dept. of Computer Science, University of Illinois, Urbana, Illinois)

Caeotron is a project in visual prostheses that derives visual information from two television cameras and outputs the information to the user, namely a visually deprived person, in the form of a modulated tone sequence. The aural picture consists of a 16 x 16 matrix matted onto the field of the television cameras, and the audio system scans this matrix picture in a way similar to that in which a television camera scans its field. Each of the 16 lines is represented in the aural picture by a distinct frequency, and each of the 16 cells of each line is displayed serially. Frequency shifts correspond to brightness variations, while an amplitude modulation of the tone corresponds to the distance of a given element.

R75-239—Hohulin, K. R., "Network Transduction Programs Based on Connectable and Disconnectable Conditions with Fan-in and Fan-out Restrictions" (50 pp., Technical Report UIUCDCS-R-75-719, Dept. of Computer Science, University of Illinois, Urbana, Illinois)

Two computer programs (NETTRA-G1-FIFO and NETTRA-G2-FIFO) which implement network transduction procedures based on connectable and disconnectable conditions with fan-in and fan-out restrictions are presented in this paper. These programs can synthesize NOR (NAND) networks with either completely or incompletely specified output functions. The results of computer experiments with NETTRA-G1-FIFO and NETTRA-G2-FIFO for both completely and incompletely specified functions are also presented.


This paper gives an algorithm to find the optimal number of pages in the working set of each program in a multi-programming system so as to reduce the total number of page faults to a minimum. It has been shown that under the assumptions specified, all programs should share the memory equally or fully allocation is done for the program whose size is less than its share.

R75-241—Stigall, P. D., "Designing and Supporting HMO, an Integrated Hardware Microcode Optimizer" (72 pp., Dept. of Electrical Engineering, University of Missouri, Rolla, Missouri)

This paper discusses an algorithm for optimizing the density and parallelism of microcoded routines in microprogrammable machines. Besides presenting the algorithm itself, this research also analyzes the algorithm's uses, design integration problems, architectural requirements, and adaptability to conventional machine characteristics. Even though the paper proposes a hardware implementation of the algorithm, the algorithm is viewed as an integral part of the entire microcode generation and usage process, from initial high-level input into a software microcode compiler down to machine-level execution of the resultant microcode on the host machine. It is believed that, by removing much of the traditionally time-consuming and machine-dependent microcode optimization from the software portion of this process, the algorithm can improve the overall process.

R75-242—Toisser, A. J., "Optimization of Some NAND-NOR Networks with Multiple Inverter" (10 pp., U.E.R. des Sciences et Techniques, Le Havre, France)

The bulk of this paper is used to tabulate the numbers of NAND- and NOR-gates required to realize disjunctive, conjunctive, or inhibited forms of logic functions; availability of multiple inverter gates is taken in account. Two modes of inhibition are considered.

R75-243—Birolini, A., "Hardware Simulation of Semi-Markov and Related Processes—Part 2: Simulation of Noise Pulses and Some Further Applications" (62 pp., Institute of Applied Physics, Swiss Federal Institute of Technology, Zurich, Switzerland)

This second part of a two part paper deals with applications of generators of semi-Markov and related processes. At first, the problem of model-building and simulation of noise pulses which occur in bursts on data channels is investigated in detail. A general classification of the models is proposed, the known models are reviewed, models based on semi-Markov processes with a hierarchical structure are introduced. The hardware simulation of noise pulses is considered for all the models treated. Generation of random test signals and some other applications in the fields of reliability and queuing theory, as well as in those of biomedical and nuclear engineering, are then briefly discussed.

R75-244—Goyal, D. K., "Parallel Evaluation of Elementary Symmetric Functions" (16 pp., Technical Report No. 184, Dept. of Electrical Engineering, Computer Science Laboratory, Princeton University, Princeton, New Jersey)

A method is presented for evaluating in parallel the elementary symmetric functions:

$$F_j(x_1, x_2, \ldots, x_N) = \sum_{1 \leq i_1 < i_2 < \ldots < i_j \leq N} x_{i_1} x_{i_2} \cdots x_{i_j} \quad 1 \leq j \leq N$$

of N elements over an arbitrary commutative ring in $O((\log N)^2)$ time using $O(N^2)$ operations. Some efficient algorithms for computing individually the functions $F_1, F_2, F_{N-1}$ and $F_N$ in time $O(\log N)$ using $O(N)$ processors are also suggested.

R75-245—Kroustalis, J. B., "On Piecewise Linear Minimax Approximations of Convex Functions" (10 pp., Research Center of National Defense, Galatsi, Athens, Greece)

This paper discusses how structured programming methodology has been introduced into a large production programing organization using an integrated but flexible approach. It next analyzes the advantages and disadvantages of each component of the methodology and presents some quantitative results on its use. It concludes with recommendations based on this generally successful experience, which could be useful to other organizations interested in improving reliability and productivity.

R75-247—Preparata, F. P. and D. E. Muller, "Efficient Parallel Evaluation of Boolean Expressions" (3 pp., Coordinated Science Lab., University of Illinois, Urbana, Illinois)

A boolean expression with $n$ literals can be evaluated by a parallel processing system in at most $1.81 \log_2 n$ steps, or, equivalently, by a network constructed with two-input AND- and OR-gates and having at most $1.81 \log_2 n$ levels.

R75-248—Belgard, R., "BLAISE-1726" (5 pp., Burroughs Corporation, Goleta, California)

Microprogramming as a valuable tool for both experimental and production products is shown through the effective realization of an alien, experimental architecture by a microprogrammable host machine. Described is the micro-implementation of the BLAISE machine on the Burroughs B1726. Some of the features of the high-level language oriented architecture are discussed with respect to implementation schemes. A structured microprogram organization is presented, illustrating the benefits of the approach.