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R75-1--Yuen, C. K., "A Theorem on the Cyclic Correlations of Walsh Functions" (5 pp., Computer Centre, Australian National University, Canberra A. C. T., Australia).

It is shown that the cyclic correlation between two Walsh functions is identically zero except if they have equal degree.


Maintenance design of telephone central offices must be integrated into the basic organization of the system. This is necessary to achieve dependability and low cost. This paper describes the maintenance design of a small processor using integrated circuit technology. It covers the basic elements of fault detection, system recovery, fault diagnosis, and repair. Although the design involves both hardware and software techniques, this paper is more concerned with the hardware aspects of the design.


The problem of scheduling tasks on a system of independent identical processors is discussed, and the performance of a suboptimal method is evaluated. The computation is modeled by an acyclic directed graph G(T, <), where node set T represents the set of tasks to be completed and edge set < defines the precedence between tasks. The objective is to minimize the finishing time of the computation graph. Known theoretical results are reviewed, and a general branch-and-bound algorithm for finding optimal solutions is presented. The schedules produced by a simple critical path priority method are shown to be near optimal for randomly generated computation graphs.

R75-4--Schank, K., "N-Graph Compaction and a Proposal for Text-Compacting Peripheral Devices" (30 pp., TRIMIS-Army, WRAMC, Washington, D.C.).

Significant compression of textual data files can be achieved by existing methods of compacting frequent n-graphs into single character codes. In addition, text compacted in such a manner can be searched and retrieved with greater facility than raw uncompacted unindexed text. Since such narrative text in ISR and data base systems is not often altered or otherwise processed significantly, it need never be re-expanded if a printer is constructed that directly prints n-graphs. Compactation utilizing the necessarily a priori known n-graphs should be possible via special text compaction hardware incorporating a fast parallel associative array. Comments and questions are included based on presentation at the Workshop on Computer Architecture for Non-Numeric Processing, 1974.

R75-5--Rajlich, V., "Parallel Programming Revisited" (25 pp., Research Institute for Mathematical Machines, Prague, Czechoslovakia).

In the paper, FORK-QUIT-EXCHANGE system for parallel programming is described. It is shown that this system is suitable for both parallel forking and parallel array processing. A machine code based on this system is described and discussed.


Specifications for a positional number system are listed as uniqueness and completeness. Uniqueness requires that only a countable set of numbers have multiple representation, and completeness requires that all numbers must be representable. The restrictions that these specifications have on the set of allowable coefficients of the system are determined, and examples from positional number systems meeting the stated requirements are given.

R75-7--Waxman, M. J., "An Approach to the Denial of Service Problem in Computer
Security” (12 pp., TRW Systems, Redondo Beach, California).

The denial of service problem of computer security is discussed. The key elements involve: identification of resources both physical and logical, determination of resource requirements, resource scheduling, resource usage monitoring, and control. A major model for service is presented. A solution approach to the denial of service problem is then given. This involves extension of the access control matrix for files to include access control for resources and time binding. The relationship to restart-recovery problems is discussed.


The analog conversion from x to sin x is achieved by using the converter from x to arc sin x in the feedback of the integrator. In this x to arc sin x conversion the averaged output signal of the comparator in which the input signal x is compared with an auxiliary harmonic signal \( A_0 \sin x \) is utilized. Converter operating in two quadrants with static accuracy better than 1% can be utilized for signals with frequencies up to 15 Hz using the auxiliary signal of frequency 1.5 kHz.


A new approach is presented for fault test generation for combinational logic. This approach combines test generation together with test evaluation and thereby reduces the required computation. For each primary input, dynamic tests are derived which consist of the comparison of two adjacent input cubics which yield different expected output values at the same output terminal. Concurrent with the generation of each test, the evaluation of the test is also performed with little computational work beyond the work necessary to generate the test. Although each test is designed to test one of the inputs to a s-a-0 or s-a-1 faults, the test evaluation yields a list of all single internal faults which are also detected by the same test. Since dynamic tests consist of the comparison of the outcomes of two static tests, the test evaluation also yields a restricted list of multiple faults which are detected by the same test.

R75-10—Usas, A. M., “The Detection of Errors in Periodic Signals” (35 pp., Stanford University, Stanford, California).

Periodic signals have a known behavior, and deviations in their waveforms may indicate failures in the signal source. Monitoring these signals can be a valuable technique in detecting both hardware and software failures in a computer. Schemes previously used to check for errors in these signals are reviewed and evaluated. These circuits, however, share a common weakness in that they are susceptible to undetectable internal faults. Described here is a self-checking periodic-signal checker; that is, the checker is capable of indicating the occurrence of any error in the input signal and failures in the checker itself. Applications of the checker in aspects of computer operation as well as a fail-safe circuit for communicating the detection of an error to an external observer are presented.


This paper develops efficient FFT programs to transform arrays of dimension N, where N can be written as a power of two possibly multiplied by arbitrary factors. Two programs were developed which use Radix-2 and Radix-4 transformations for the binary factors. These programs call another subprogram to transform with respect to the arbitrary factors, if any. Since the sequential transformation is well known, the emphasis is on developing an efficient unscrambling procedure to follow the transformation. The factors of N are arranged symmetrically with respect to a pivot which is either an imaginary line or a product of all the nonsymmetric factors. Then, the unscrambling is performed in one step by moving along closed loops, directly to the desired locations, those elements that are not stored at the proper address. The computation of the loops requires very little auxiliary storage. Formulas are given for the number of multiplications, additions, and transfers. The transformation is very efficient, except that the transformation with respect to the arbitrary factors could be made faster if one is willing to write a special program for each factor. The unscrambling procedure remains efficient even when many arbitrary factors are involved.

R75-12—Mathur, F. P. and P. T. de Sousa, “GMR: General Modular Redundancy” (75 pp., University of Missouri, Columbia, Missouri).

This work presents the concept and analysis of General Modular Redundancy (GMR) as a general model suited for both static and dynamic redundant structures. This model subsumes in its generality all other known models of redundant structures. In addition to the synthesis of existing models, new models are also developed and analyzed, such as the NMR Hybrid system with standby spares where the NMR core units are subject to stuck-at-0, stuck-at-1, or stuck-at-X failures and where failures may occur in a mutually compensatory manner.

R75-13—Rhine, V. T. and P. S. Nee, “Minimum-Cost Excitation of the Delay Storage Element” (13 pp., Texas A and M University, College Station, Texas).

The synthesis of a sequential system involves the generation of the excitation equations for the storage elements that it is to use. For the delay storage element (including the D flip-flop), an unusual degree of freedom is allowed in that either the excitation signal or its complement can be used to control the storage element, with no loss of generality. This freedom always allows the implementation of any excitation in the most minimal two-level form unless additional restrictions are placed upon the designer.


The problem of job scheduling in a computing system containing processors of different operation speeds is studied. In particular, bounds on the worst case performance of some scheduling algorithms that can be implemented easily are obtained. Such bounds also provide us with information concerning the effect of the speeds of the processors and the maximum throughput of the system on the performance of these scheduling algorithms. The trade-off between the speed and the number of processors in the system is also discussed. Optimal scheduling algorithms (31 pp., in the ILLIAC-3 room of the University of Illinois. This computer is currently used to control the various picture processing peripherals in the room as well as routing information to the general purpose computer IBM 360/75.) for processing. The following paper describes the usage and design principles of the operating system in coping with the above environment.


A multiprogramming (semi-) virtual memory operating system has been written for the minicomputer PDP 8/3 located in the ILLIAC-3 room of the University of Illinois. This computer is currently used to control the various picture processing peripherals in the room as well as routing information to the general purpose computer IBM 360/75. The system is described here. The following paper describes the usage and design principles of the operating system in coping with the above environment.


The solution of some industrial process control problems can be expressed as a system of Boolean algebra equations using variables representing inputs from and outputs to the real world. If this system is solved sequentially, cyclically, and in real time, the outputs may be used directly to

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control the state of real world devices. VIPTRAN2 is a high-level FORTRAN-like language which allows the programmer to express his Boolean system symbolically in logical (Boolean) equations. The VIPTRAN2 compiler reduces the input to machine code for the VIP process control. The result is an intellectual tree as a relay tree. The concept is extensible to other industrial controllers.


CLEOPATRA is a general purpose and systems implementation language in the style of ALGOL designed for computers similar to the IBM System/360. Among its concepts are extensions to the ALGOL block structure, user-defined data types and data access mechanisms, and user-defined "generic" operators. The language is goto-free, and has a generalized decision table as its main control structure. An interrupt mechanism is proposed. The report attempts to define a new language. It is intended as a user's manual for a prospective implementation.


Given a set of objects each described by a vector of characteristics, a clustering technique groups those objects with similar characteristics together into subsets called clusters. The similarity criterion uses an appropriate distance function measuring the distance between objects which varies with the interpretation of the characteristic vector for the set. Clustering techniques are useful in many areas. For example, they can be used in medicine to identify new diseases and to refine existing disease categories, in biology to develop taxonomies for plants and animals, and in archaeology to classify artifacts with respect to period and style. In clique generation a cluster is defined to be a maximal complete subgraph or clique of the graph. A complete subgraph is one in which every node in the subgraph is adjacent to every other node in the subgraph. A maximal complete subgraph is a complete subgraph which is not properly contained in any larger subgraph. The problem of finding all the cliques in an arbitrary graph is well known, and many algorithms have been proposed. Cliques contain more information about the structure of a graph than connected components, and although they are often too tight to be used as clusters, they can form the nuclei of useful clusters. Hence we will restrict our attention to clique generation. We first present a detailed study of the Bron-Kerbosch algorithm. The algorithm is described, analyzed, and shown to be near optimal. Then we discuss the efficient implementation of the algorithm, describe an efficient new implementation, and present numerical results demonstrating the superiority of the new implementation over previous ones.


An experimental retrieval system designed to support data bases with little inherent structure is described. The initial data base consists of the full text of several technical articles on information retrieval. Searching proceeds by means of a direct sequential scan through the data, and the user has very general control over the structure and context of the search. The system runs on a micromprogrammable minicomputer, and several text searching and manipulation commands have been implemented in microcode. Part I of the report is a user's guide. Part II contains detailed technical descriptions of algorithms employed for parsing, scheduling, and executing a search request. The system will be used to analyze strategies for efficient searching in this environment and to study the interaction between the system and a group of motivated users under controlled conditions.


A BASIC language interpreter has been designed for use in a microprocessor environment. This report discussed the development of 1) an elaborate text editor and 2) a table driven interpreter. The entire system, including text editor, interpreter, user test buffer, and full floating point arithmetic routines fits in 16K words.


Two approaches to data compression in a telecommunications environment are examined: contiguous duplicate character compression and common phrase detection/replace. Algorithms for each method are presented. Each method is shown to be useful for a given class of transmitted messages.


This report discusses the current state-of-the-art in computer recognition of handwritten characters. Several current schemes are examined and criticized. A new recognition method is developed utilizing a vocabulary gradient tablet for input and clever software for essential feature extraction. A simulation program is included as an appendix.


The PLW language and the structure of the first PLW compiler, done in assembly language and FORTRAN is detailed herein; the compiler has been written in PLW itself. The PLW language is in many respects like PL/I. The object language of the compiler is FORTRAN. Hence the compiler code is, to a great extent, portable.


RECURSE is a lesson for the PLATO IV computer-based education system. It attempts to give the student a general feel for recursion and introduces him to the use of recursion in recursive definitions and recursive procedures. This report contains a description of the lesson and its development, and a listing of the TUTOR source code.


pl/2d is a recursive mini-language which produces a graphical output. The languages allow the student to “see” how recursion works. The motivation for the design was to produce a useful tool that is easy to use and isolates the topic of recursion.


The need for easy to use statistical systems has grown rapidly in recent years. Interactive Express Statistical System (INESS) combines the fast turnaround of the Express job system with the conversation capabilities of Call-OS FORTRAN on the IBM System/360 time-sharing system to provide an instructive and easy to use tool for many statistical analyses. This paper deals with design considerations during the development of INESS, with emphasis on the implementation language and interaction between the PL/RTS and Express systems. Examples of usage, sample segments of code and message file structures are taken from the Correlations-Factor Analysis statistical area.


The paper is addressed to learning processes which employ inductive inference. A system of variable-valued logic, called V/L, is briefly described, and its application to implementing inductive learning processes is discussed. The V/L can be characterized as a "multi-valued first order predicate logic." An example is given of learning by a computer program the difference between two classes of objects.