
Complete documentation is provided for SURGE717, a non-proprietary computer program which generates appropriate data-processing logic and produces COBOL source programs from simple descriptive parameter cards. This machine-independent and application-independent software package provides programmer and non-programmer personnel with a shortcut approach to file sorting, selective retrieval, and tabular report generation, including multiple levels of totals and a capability for certain other kinds of computation. The machine-generated COBOL coding is intended primarily for direct use, but also as a skeletal source program for possible modification. In either instance, the purpose is to achieve a uniformity of program logic and to reduce significantly the time consumed by laborious coding and logic design. This report provides both non-technical user directions, and technical documentation of the internal workings of the package as well as suggested installation procedures. Included in this 223-page report are a variety of illustrations, a complete listing of the generator program, references to 14 items of related literature, and a 530-item page index.


This document is the current issue of the Abstracts of Computer Literature formerly contained in the pages of the Transactions on Computers, and now available for the Computer Society Repository. The format and description is unchanged, including the abstracts themselves, the descriptor-in-context index, the identifier index, and the author index. This will be a monthly feature of the Repository. Price: Photocopy — $3.50 each ordered individually; $30 for a year’s subscription. Microfiche — $2.50 each ordered individually, $24.00 for a year’s subscription.


The MULTIGAP is an extension of the segment gap structure provided in the Western Electric string language processor which permits full mimicking of built-in functions, arbitrary number of arguments in lists, and reduces script and actual computation required for tasks in which it is used.

disjunctive networks possess the interesting property that all networks of c cells realize the same number of functions (but not necessarily the same functions). Further, it is shown that all disjunctive networks of c cells realize the same number of functions dependent on all input variables.

R73-72 Bondi, J. O., and Stigall, P. D. “Decimal-Base Binary Logic (DBBL) Adders and Registers.” (78 pp.; University of Missouri, Rolla, Mo.)

This paper discusses a new type of base n adder and storage register. This new type of logic is called “n-base binary logic”, or NBBL. The NBBL system is compared and contrasted with the Post base n system (a type of n-valued logic), the binary-coded base n system, and the straight binary system. The main purpose of this paper is to show that a decimal, or base 10, system can have some important inherent advantages over a binary system, such as greater daily operational efficiency. Furthermore, it is shown that a “decimal-base binary logic” system, or DBBL system, has inherent advantages over the Post and binary-coded decimal systems. A cost analysis of the DBBL system relative to the straight binary system is performed and several circuit realizations for general NBBL adders and storage registers are shown. Two of the storage register realizations are SCR models that the author has actually built and thoroughly tested.

R73-73 Huskey, H. D. “The Polish Assembler.” (32 pp.; University of California, Santa Cruz, Cal.)

In the development of a Video Terminal System at the University of California at Santa Cruz it soon became apparent that a resident assembler would expedite the development of the system programs that were needed. Typically, assemblers have been developed for larger card-oriented systems. These systems have been taken over intact for small computers, and the optimization valid for their card systems is not valid for the small systems. Therefore, a system was developed with the following characteristics:
  1) it was to remain resident in core while compiling major programs, 2) the object code was to be re-entrant since a time sharing system was being developed, 3) the language was to use the ASCII character set, 4) it was to be format free, and 5) it was to compile fast enough so that there would be no incentive to keep the programs in object form. To accomplish this it was convenient to reverse the usual assembler format of (op code) (operand) into (operand) (op code). This structure led to the name Polish Assembler, or PASS, since the

In an electronic analog computing system, the accuracy of nonlinear voltage transfer functions can be improved by taking advantage of the nonlinear behaviour of certain non-ohmic resistive networks. As a result it is reasonable to generate fractional power approximations of desired functions, utilizing the applicability of this approximation for uniformly continuous non-linearities. In this paper the fractional power approximation is introduced, as well as a discussion of how the optimum approximation of the given function is determined. Also it is shown both theoretically and experimentally how various elementary nonlinear functions can be properly approximated and accurately produced.

R73-75 Ercueu, J. "Location of Single Faults in Combinational Circuits." (16 pp.; Laboratoire d'Automatique, Toulouse, France.)

This paper presents a systematic method for establishing test sequences for the location of single fault in a switching network. The method is purely Boolean and is based on observability of logical states. First an algorithm establishing a single fault detection sequence is briefly described. Then the definition of single faults equivalence classes is given which is appropriate for computer use and which allows to establish a fault location test sequence.


This paper presents an algorithm for the shift register realization and/or decomposition of a linear sequential machine under similarity transformations. In this way both minimality and independence of starting state are preserved. The algorithm uses the fact that a shift register realization and machine decomposition correspond to a canonical form of the state equations. The general algorithm includes algorithms for obtaining the family of similarity transformation matrices \( \mathcal{F}(M) \) that transform the state transition matrix into a similar canonical matrix form. Finally the algorithm selects those similarity transformations which satisfy the additional requirements of shift register realizability and/or machine decomposition.


This paper investigates a new approach to the reliability analysis of logic circuits. An efficient algorithm for computing the reliability matrix of a sequential (or combinational) logic network whose components are characterized by a known probability of malfunctioning is presented. Using the concept of path sensitizing, a graphical representation for the propagation of errors in a logic circuit is derived. Through the computation of Boolean path functions, the set of error propagation graphs is formulated in the form of a multifunction table from which the entries of the reliability matrix are directly computed. The method not only offers computational efficiency, but also provides further physical insight into the reliability problem.


This paper describes a novel implementation scheme for the operations of addition and subtraction in residue number systems. The method is based on the property that the set of residues modulo \( m \) form a finite group under addition (mod \( m \)). Therefore, any row in the modulo \( m \) addition table is simply a permutation of the elements of any other row. The effect of this on the implementation scheme is: The set of residues modulo \( m \) (0 to \( m-1 \)) are held in a register. For operands \( X \) and \( Y \), \( X \) is used to permute the contents of the register and \( Y \) is used to select the appropriate part of the register to be gated into the sum register. Two adder realization schemes are proposed. The first one offers higher speed but increases in complexity as the modulus size increases. For large modulus size the second scheme offers less complexity at reduced speed. By defining subtraction in terms of complement addition, subtraction can be implemented in a manner similar to the implementation of addition. The proposed residue adder/subtractor structure is very systematic and, hence, suitable for MSI/LSI realization.

R73-79 Wee, W. G. "On Reconstruction of Ambiguous Patterns." (25 pp.; University of Cincinnati, Cincinnati, Oh.)

In this paper, a number of algorithms are developed related to the reconstruction of ambiguous patterns using the x- and y-projections. Algorithm I identifies the unambiguous subpatterns of a similar pattern, while Algorithm II detects and reconstructs the unambiguous subpatterns from its projections. Properties found in a completely ambiguous pattern and relations to previous results are explained. A method to compute the number of similar patterns is also outlined.

R73-80 Diaz, M., Jeffs, J. C., and Courvoiser, M. "On-Set Realization of Fail-Safe Machines." (17 pp.; Laboratoire d'Automatique, Toulouse, France.)

Fail-safe sequential machines are such that if a failure happens in the sequential part, the proper functioning of the machine must carry on outside the code chosen to represent the set of states. This paper presents a systematic and algorithmic method to compute a single Boolean term with a don't care function for each fault. The don't care function is the same for all faults.

R73-81 Maristas, D. G. "A High Speed and Accuracy Digital Gaussian Generator of Pseudorandom Numbers." (44 pp.; Greek Atomic Energy Commission, Athens, Greece.)

In this paper a procedure for forming high accuracy Gaussian distributed pseudorandom numbers is presented, and a digital system which mechanizes the procedure is suggested. A formula describing the output of the system is derived, and tabulated results are presented. The system can be considered as a peripheral device of a general purpose machine in simulation studies, as well as in all fields where high accuracy Gaussian noise generation is required.

R73-82 Rubin, F., "The Lee Path Connection Algorithm." (40 pp.; IBM, Poughkeepsie, N. Y.)

The Lee path connection algorithm is probably the most widely used method for finding wire paths on printed circuit boards. In this paper it is shown that the original claim of generality for the path cost function is incorrect, and a restriction, called the path consistency property, is introduced. The algorithm holds for those path cost functions having this property. Codings for the cells of the grid are proposed which will allow the correct operation of the algorithm under the most general path cost function, using the minimum number of states possible, six states per cell. Then methods for reducing the number of states by increasing the number of states are presented. Storing computed cell masses is introduced as a method for reducing the amount of calculation for each iteration of the algorithm. Adding the distance from the goal to the path cost function, and expanding the most recently encountered cell, are shown to substantially reduce the number of iterations needed.

R73-83 Kaliski, M. E. "A Characterization of Isolated Finite State Machines in Terms of Planarity." (7 pp.; City College of New York, New York, N. Y.)

Isolated finite state machines are examined from the viewpoint of the theory of finite directed graphs. It is shown that the state diagram of an isolated finite state machine is necessarily a planar directed graph. The converse result is not true.

R73-84 Kamal, S., and Weinberg, B. "Diagnostic Test Selection." (9 pp.; Wayne State University, Detroit, Mich.; Michigan State University, East Lansing, Mich.)

A method for finding minimal tests to diagnose a single fault is given. A requirement is imposed that at least one test of a test set indicates whether or not the fault is present. The problem is formulated as simplifying a single Boolean term with a don't care function for each fault. The don't care function is the same for all faults.

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