The Computer Society annual conference gets a new name and a new role as THE conference on computer system design and engineering.

COMPON, the new title of the IEEE Computer Society Annual Conferences, has chosen as its continuing theme, “Innovations in Computer Systems Design.”

COMPON is introducing several innovations in conference formats and is also borrowing some procedures pioneered by other highly successful technical meetings such as the International Solid State Circuit Conference and the SHARE Conferences. Although COMPON’s purpose is to encourage a meaningful technical interchange of information between professionals on recent system designs, it plans to accomplish this in a more direct, less formal manner than the presentations at large, general conferences. It will be THE conference for computer systems engineering, both in hardware and software development.

The planned modifications will center on the conference format itself. According to Rex Rice, chairman of the COMPON Steering Committee, “Speakers are encouraged to tell what really happened (i.e., what went wrong) and what they would do differently next time in an informal presentation.” He adds, “Speakers presenting exceptionally interesting topics on continuing projects will be invited back another year to fill in the next installment.”

At the organizational level, the Governing Board of the IEEE Computer Society has created a COMPON Steering Committee, headed by Rex Rice, to establish conference policies. The purpose of this committee is to insure year-to-year continuity of COMPON. To accomplish this, the Steering Committee proposes to maintain a high caliber and large number of contributors on its Technical Program Committee. This large, semi-permanent committee will provide an excellent selection of material to the Annual Conference attendee, with a wide variety of choices for professionals in scientific, educational and industrial fields. It will glean material from workshops and conferences and contact peers all year long for suitable topics.

The Standing Steering Committee will appoint the COMPON Chairman some 18 months prior to the date of the Conference. The Chairman, in turn, will appoint the COMPON Annual Committee, whose job it will be to handle the business of putting on the Annual Conference. A semi-permanent administrative staff has been established to handle local arrangements, publicity, publication, etc., leaving the Chairman and his committee free to concentrate on the technical aspects of the conference.

Aside from the organizational level, several additional innovations are being introduced and have been included in COMPON’72 and COMPON’73. To assure continuity, a permanent conference location (San Francisco) and a standard time of year (end of February and the first of March) has been set.

Other changes include dispensing with the formal, standard luncheon format and substituting two late afternoon cocktail parties to encourage person-to-person communication, and an evening panel session where experts present their positions and may be queried by the audience.

Although a conference digest will be published, the conference will provide technical information to those in attendance that simply cannot be obtained from reading the proceedings or other literature. For example, on the fourth day of COMPON’72, a one-day course on “Semiconductor Memories” will be taught by Dr. David Hodges of the University of California. This is a professionally directed educational program that promises to be of wide interest.
INNOVATION AND CHANGE IN COMPUTER DESIGN

COMPCON72

SIXTH ANNUAL IEEE COMPUTER SOCIETY INTERNATIONAL CONFERENCE
JACK TAR HOTEL, SAN FRANCISCO, CALIFORNIA • SEPTEMBER 12-14
keynote speaker
Dr. Robert N. Noyce's contributions led to the development of the revolutionary integrated circuit industry. His latest work, involving integrated functional elements, has been assessed by many as being equally revolutionary in its impact on future architecture. This work can well change the entire economic structure of the computer industry. From this unique perspective, Dr. Noyce has agreed to share his observations with those of us involved in computer systems design. He in turn has expressed interest in establishing a constructive dialogue with system designers to better evaluate new applications of this pervasive technology. Currently President and Director of Intel Corporation, Dr. Noyce was one of the founders of Fairchild Semiconductor in 1957 and advanced in that corporation to become Group Vice President by 1965, responsible for 15,000 employees. He is the holder of 16 patents on semiconductor methods, devices and structures and has been instrumental in the development of diffused silicon devices. Elected to membership in Phi Beta Kappa at Grinnell (Iowa) College, he earned his Ph.D. in Physical Electronics at Massachusetts Institute of Technology. Dr. Noyce is a member of the National Academy of Engineering, an IEEE Fellow and a member of the American Physical Society.

DR. ROBERT N. NOYCE

technical program chairman
Dr. Algirdas Avizienis, Professor and Vice Chairman of the Computer Science Department of the University of California, Los Angeles, was educated through the Ph.D. in electrical engineering at the University of Illinois, Urbana. While a fellow and research assistant at Illinois, he participated in the design of the ILLIAC II computer. As senior engineer at Pasadena's Jet Propulsion Laboratory in computer systems research, he initiated the JPL Self-Testing-And-Repairing (STAR) Computer research project. He has remained as principal investigator for the STAR project since joining the faculty at UCLA in 1962. In connection with this work, he received the NASA Apollo Achievement Award in 1969. For organizing and chairing the first workshop on the Organization of Reliable Automata, he received the IEEE Computer Society Honor Roll Award in 1968. He organized the Technical Committee on Fault-Tolerant Computing and has served as its chairman since 1969. In 1971 he was General Chairman of the first International Symposium on Fault-Tolerant Computing. Dr. Avizienis, a native Lithuanian, is a member of Sigma Xi, Tau Beta Pi, Eta Kappa Nu, the ACM and of the Governing Board of the IEEE Computer Society.

DR. ALGIRDAS AVIZIENIS

compcon 72 chairman
Tracy S. Storer has been active for almost two years in his chairmanship of the Sixth Annual IEEE Computer Society International Conference. He is Vice President, Product Development, of Time/Data Corporation, a General Radio Company, Palo Alto. Storer was instrumental in the creation and adoption of the name COMPCON to designate this and all future annual Computer Society conferences. The Chairman received the BSEE from Cornell University and earned his MSEE at Stanford University, followed by advanced study at the Stanford Graduate School of Business. At Hewlett-Packard in Palo Alto, Storer spent 11 years. He was instrumental in the development of the HP 5243/5 family of electronic counters, led HP's entry into nuclear instruments and digital signal processing, and from 1968 to 1971 managed Hewlett-Packard's computer design operations. Before being named to lead the organization and activities of Compcon 72, he was active in various ACM, IEEE and Computer Society affairs.

TRACY S. STORER
**program sessions**

**STAR-100**
CHAIRMAN: S. Fernbach, Lawrence Livermore Lab
The CDC STAR-100 computer is a pipeline processor structured around a 4 million byte high bandwidth memory. Instructions specify operations on streams of data allowing full use of the memory bandwidth and the arithmetic pipelines. In streaming mode, the system can produce 100 million 32-bit floating point results per second.

CDC STAR-100 Processor Design: R. Hintz, D. Tate, CDC, St. Paul
Implicit Storage Management: P. Jones, CDC, St. Paul
STAR: A De-education Problem: L. Krider, CDC, Palo Alto
A System Programmer's View: J. Requa, Lawrence Livermore Lab

**SYMBO: A UNIQUE ARCHITECTURE**
CHAIRMAN: R. Rice, Fairchild Systems Technology
This research computer combines the direct hardware implementation of a high-level language in large, two-layer, printed circuit boards in a high-speed packaging environment. Key features presented are the hard-wired time sharing supervisor algorithms and the hardware packaging. The SYMBOL machine, in use at Iowa State University, demonstrates the impact of SYMBOL philosophies on system architects and architecture.

A Project Overview: R. Rice, Fairchild Systems
System Supervision Algorithms: W. Smith, Fairchild Systems
The Hardware Implementation: R. Rice, Fairchild Systems
The Operational Aspects: Zingg & Richards, Iowa State U.
Significance of the Project: Y. Chu, U. of Maryland

**INNOVATIVE PROCESSORS**
CHAIRMAN: Y. Chu, U. of Maryland
The clever use of existing components with new techniques of multiprogramming and array processing can produce impressively powerful computer systems. New programming techniques using higher level languages can greatly reduce programming cost and make these powerful systems easier to use.

Implementation of a Higher-level Language on an Array Machine: A. Avizienis and M. Vineberg, UCLA
Fast Computers from Slow Parts: D. Kuck, U. of Illinois, and Y. Muraoka, Nippon Tel & Tel
A Multiprogrammed Highly Parallel System: Ben-Zion Barta, Israel

**PEPE: A PARALLEL PROCESSOR**
CHAIRMAN: G. Bergland, Bell Labs, Naperville, Ill.
PEPE: (Parallel Element Processing Ensemble) is a highly-parallel computer designed to augment a conventional sequential computer in the radar data processing application. A large number of identical processing elements operate in parallel under common control. The elements of the ensemble are used to form a data base which can be updated in parallel and searched associatively.

Architecture: G. Crane, M. Gilmartin, J. Huttenhoff, P. Rux and R. Shively, Bell Labs, Whippany
Support Software System: D. Wilson, Bell Labs, Whippany
System Applications: G. Bergland and C. Hunnicutt, Bell Labs, Whippany
Parallel Processing of BMD Radar Data: J. Cornell, SDC, Huntsville

**DESIGNING WITH MOS-LSI**
CHAIRMAN: R. Walker, Fairchild Semiconductor
Many parallels may be drawn between computers on a chip and the early days of computers. The real-life world of custom MOS-LSI is beset with difficulties and obstacles that the semiconductor houses seldom discuss.

HP Mod 35 Pocket Computer: T. Whitney, HP, and R. Paleck, MOSTEK
A Universal Microprogramming Controller: J. Stanford, MM, and R. Hansen, Fairchild
From Calculators to Computers with LSI: A. Prophet and N. Grannis, AMI

**DIGITAL ARITHMETIC**
CHAIRMAN: H. L. Garner, University of Pennsylvania
The most outstanding papers of general interest from the symposium on computer arithmetic at the University of Maryland have been selected. There are new algorithms and hardware implementations of arithmetic for computer systems.

Control of Errors in Binary Computing: N. Metropolis, Los Alamos Sci. Lab
Redundancy in Computer Arithmetic: D. Atkins, Univ. of Michigan
Automatic Computation of Exponentials, Logarithms, Ratios and Square Roots:
T. C. Chen, IBM, San Jose
Pipeline of Arithmetic Functions: M. Flynn, Johns Hopkins U.

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*the system design professional's conference*

"Innovative Computer Architecture" is the principal focus for COMPCON 72. The topics are arranged into four sub-conferences, totaling 16 sessions which permit breadth or depth coverage as your professional interests dictate. These are:

- Case Studies of Major Computer Systems
- Computer Subsystems and Technology
- System Analysis, Design Tools and Performance Measurement
- Evolving Computer Architectures

The papers represent selections from six workshops and symposia held during the past year as well as a large response to the call for papers. In addition to the usual after-hours technical discussions with peers, the conference attendee will obtain, through the structured interactive sessions, a great amount of rich detail which cannot be included in the Conference Digest. This conference provides the opportunity for interaction, allowing you to gain the benefits you have every right to expect from a meeting of professionals.
ANALYSIS & ARCHITECTURE
CHAIRMAN: R. D. Hunter, Burroughs Res. Ctr., La Jolla
Microprogramming has become an accepted approach in the implementation of computing system architecture. New techniques have been developed for designing microprograms, self-checking features, using microprogramming in a scheme of achieving parallel processing, and design considerations and trade-offs in micro-programmed computers.

MDS (Microprogram Design System) Translator — An Introduction: E. Dubbs, R. Parsons and J. Petersen, IBM, San Jose
Design of Self-checking Microprogrammed Switching Processor: H. Chang, Bell Labs, Naperville
SIMDA — A Microprogrammed Parallel Processor: A. Wester, Texas Instruments
Some Design Considerations of Cache Memories: H. Barsamian, NCR, Hawthorne
Analysis of Trade-offs Considerations in Microprogrammed Computers: C. Rama-moorthy and M. Tsuchiya, U. of Texas, Austin
A Method to Model Microprograms and Analyze Their Behavior: G. Baliliu and D. Ferrari, UC Berkeley

THE ROLE OF MEMORIES IN COMPUTER ARCHITECTURE
CHAIRMAN: W. W. Chu, UCLA
Memory system design is one of the most important aspects of computer architecture. The advance of semiconductor and magnetic storage technologies along with new methods for dynamic data allocation make this subject one of the fastest changing areas of computer design.

Memories and the Silent Revolution in Systems Architecture: H. Kurpanek, ITEL Corp.
Mixed-Mode and Multidimensional Memories: E. D. Jensen, Honeywell, St. Paul
Microcache: A Buffer Memory for Microprograms: A. Robbi, RCA, Princeton, N.J.
Applications of Some Switching Network Results to Dynamic Allocation of Memories in a Hierarchy: D. Gold, U. of Illinois
Interconnection Networks for Processors and Memories in Large Systems: D. Kuck and D. Lawrie, U. of Illinois, and Y. Murakoa, Nippon Tel & Tel

THE IMPACT OF TECHNOLOGY ON ARCHITECTURE
CHAIRMAN: R. A. Henle, IBM
The rapid evolution of computer technology has made possible new classes of components with greatly increased functional capability. These changes affect the logic and design of evolving computer systems.

Which Logic Technology for MSI and LSI Systems?: D. Hodges, UC Berkeley
Providing Non-Volatile LSI Memory: D. Appelt, Texas Instruments
The New LSI Components: T. Hoff, INTEL
Storage Hierarchy Design: R. Mattison, IBM, San Jose

ANALYSIS OF COMPUTER SYSTEMS
CHAIRMAN: R. Mattison, IBM, San Jose
Computer system analysis and optimization techniques enhance our understanding of subsystems such as storage, complex configurations like multi-processors, and other problems of computers communicating. System models, goodness criteria, and optimization techniques are required to analyze these problems.

I/O Subsystems with Seek-Type Direct Access Devices: T. Manocha, IBM, Kingston
Optimization of Centralized Interactive Networks: H. Najjar, IBM, Gaithersburg
Multiprocessor Control with Partial Program Memory Replication: A. Covo, GTE
Sylvania, Needham Heights
Network Message Routing by Mathematical Programming: D. Cantor and M. Gerla, UCLA
Scheduling Unidentical Processors in a Stochastic Environment: K. Chandy and J. Dickson, U. of Texas, Austin

THE LOGOS SYSTEM
CHAIRMAN: E. L. Glaser, Case Western Reserve Univ.
LOGOS is a design environment created by a small team of designers at interactive consoles where a total design of operating systems and hardware of a system can be created by a combination of algorithms and user interaction.

Introduction of and Overview of LOGOS: E. Glaser, CWR U.
State of Hardware/Software Design: F. Heath and C. Rose, CWR U.
A LOGOS Design Scenario: A movie
LOGOS Representation: C. Rose and F. Bradshaw, CWR U.
LOGOS — Where it is and Where it is Going: E. Glaser, CWR U.

COMPUTER PERFORMANCE MEASUREMENTS
Chairman: V. Cerf, UCLA
A wide range of methods for systems design of enhancements, and studying the degree must be understood in order to design better. This can be accomplished through performance modeling.

The Systems Performance and Design Evaluations Display System: W. McClelland, ARPA
A Multipurpose Processor-Enhancement Design Evaluation: UC Berkeley
Selected ARPA Network Measurement Equipment

LANGUAGES FOR DESIGN
CHAIRMAN: G. Bell, Carnegie-Mellon Univ.
The development of large complex systems is becoming more difficult without a language to describe instruction sets. The creation of architecture can be greatly aided by a
PMS: A Notation to Describe Computer Architecture
ISP: A Language to Describe Instruction Sets
M. Barbacci, G. Bell and A. Newell, Carnegie-Mellon
Introducing the Computer Design Language Description and Realization of Digital Systems
The Best Language — A Language for Use by theorists and R. Tulloss, Western Electric,
at a glance

SYSTEM ANALYSIS, DESIGN TOOLS & PERFORMANCE MEASUREMENT

10. ANALYSIS OF COMPUTER SYSTEMS

11. THE LOGOS SYSTEM

12. COMPUTER PERFORMANCE MEASUREMENT

13. LANGUAGES FOR DESIGN

14. SIMULATION TEST AND DIAGNOSIS

EVLING COMPUTER ARCHITECTURES

15. ADVANCES IN SYSTEMS ARCHITECTURE

16. PARALLEL PROCESSORS

17. MODULAR COMPUTERS

18. FAULT-TOLERANT ARCHITECTURE

the future of professional societies in computer science and engineering

12

reception

13

panel discussion #3

14

social hour

15

Modular Computer Systems: R. Ellis, Washington U., St. Louis

Register Transfer Modules (RTMs) for Understanding Digital Systems Design: G. Bell, J. Grason and D. Siewiorek, Carnegie-Mellon U.

The Promise of Macromodular Systems: W. Clark and C. Molnar, Washington U., St. Louis

High Level Logic Modules: A Quantitative Comparison: R. Ellis and M. Franklin, Washington U., St. Louis


16

Design for Fault Tolerant Computation

CHAIRMAN: J. Goldberg, SRI

A decade of work has been invested in the art of designing fault tolerant computers. The major emphasis has been on stringent applications, such as space and the telephone systems. The next decade will see a proliferation of applications that will require our best efforts in applying existing techniques and developing new ones.

Experience and Experiments with the JPL Star Computer: A. Avizienis and D. Rennes, JPL, Pasadena

Design for Detection: An Attempt at Complete Fault Diagnosis of a Store: F. Goetz, BTL, Naperville

A Prognosis on Fault-Tolerant Digital Control Systems: A. Hopkins, Jr., MIT

Reliability of Modular Computer Systems with Varying Configuration and Load Requirements: J. Bricker and W. Martin, Hughes, Fullerton
McDowell award

Dr. Jean A. Hoerni, Chairman of the Board of Directors of Intersil, Inc., will be presented the 1972 W. Wallace McDowell Award during opening ceremonies of COMPCON 72. The award was voted to Dr. Hoerni "for significantly influencing the architecture and design of data processing systems by inventing the planar process of semiconductor circuit fabrication—the development that made possible the economical mass production of reliable integrated circuits and semiconductor memories."

ladies' programs

A complete three-day program of activities has been organized for the wives of COMPCON 72 attendees, beginning with a Tuesday coffee from 9:00 a.m. until 1:00 p.m. in Suite 378 of the Jack Tar Hotel. A deluxe tour of The City is scheduled for 1:00 p.m., which will return in time to prepare for the party Tuesday evening. Wednesday at 9:00 a.m., a continental breakfast will be served in Suite 378, after which small groups will be conducted on a visit "behind the scenes" in some of San Francisco's loveliest shops, including Gump's, I. Magnin, F.A.O. Schwartz, Dunhill of London and many more. Comfortable shoes are advised. Thursday at 9:15 a.m., a cab excursion leaves for Fisherman's Wharf, a visit highlighted by a cruise of San Francisco Bay. Upon landing, you will stroll through the charming shops of the wharf, the enchanting Cannery and world-famous Ghirardelli Square. You will return to the hotel after lunch via the famous San Francisco Cable Car.

"the city:"
San Francisco

September, with its mild days and cool nights, is the most weather-perfect month in San Francisco, offering soothing relief to visitors from other parts of the country. Rain is almost unknown, and the fog obligingly confines itself to early morning hours (if it appears through the Golden Gate at all). Though September is the most beautiful month in The City, U.S. Department of Commerce figures show San Francisco as one of the three sunniest cities in the nation the year round.

WHAT TO WEAR: The nights can be nippy, so come prepared. Women favor lightweight wools or orlon knits for daytime, with suits ideal for adapting to the temperature changes. A lightweight coat would be smart (in every sense of the word), and fur jackets and stoles are seen on San Francisco streets all year. Head scarves are wonderfully handy, hats optional and gloves de rigueur. Men generally wear light-to-medium weight business suits of a somewhat conservative cut, with medium-weight sports jackets and slacks for casual wear. And if you forget everything else, be sure to bring a comfortable pair of shoes (a must for tramping up hills and through The City's many shop-filled, cobble-stoned alleyways).

WHAT TO DO: Hundreds of books have been written on the delights and attractions of San Francisco, and much still remains unwritten. Suffice to say that the fresh, invigorating ocean air will make you want to be on the go—to ride the cable cars, explore Chinatown, see colorful Fisherman's Wharf, the beautiful bridges, parks and scenic views and to climb to the very top of The City and look out and down upon one of the most breathtaking panoramas of the world, that of Baghdad-by-the-Bay, San Francisco.

Program Creation: THE WARR DEPARTMENT, PALO ALTO
Design: DIANE CHAPMAN
I enclose my check, payable to Regents, University of California, or authorize charge to my BankAmericard Account No. for enrollment in the Semiconductor Memories tutorial on Friday, Sept. 15 in San Francisco.

Name

Address

Daytime phone and extension

PLACE: Jack Tar Hotel, Geary and Van Ness Avenue, San Francisco
TIME: 8:30 a.m.-4:30 p.m., Friday, September 15, 1972
TEXT: SEMICONDUCTOR MEMORIES, D. A. Hodges, Editor; IEEE Press, August 1972
FEE: $60 for COMPCON 72 registrants includes luncheon and text
$70 for others

Advance registration closes August 25, 1972. After that date, registration will be accepted at the COMPCON 72 registration desk at the Jack Tar Hotel.
Please make your check payable to "COMPCON 72" and mail to:

Jan Saindon
H98 - 028
Monterey and Cottle Roads
San Jose, Calif. 95114

Name

Company

Address

City/State/Zip

ADVANCE RATES FOR COMPCON 72
(Please check appropriate box and return with your check.)

IEEE COMPUTER SOCIETY MEMBER $40.00
(Please include your membership number)

NON-MEMBER . . . . . . . $50.00

STUDENT . . . . . . . . . . . . $15.00

IMPORTANT: INCLUDE YOUR CHECK AND THIS REGISTRATION FORM IN AN ENVELOPE AND RETURN TO JAN SAINDON AT THE ABOVE ADDRESS NO LATER THAN AUGUST 25, 1972 TO TAKE ADVANTAGE OF THE REDUCED ADVANCE REGISTRATION RATE.

Please reserve ________ room(s) of the type and rate checked.

*Arrival Date ________ AM □ PM □ Departure Date ________ AM □ PM □

Name

Address

City________ State________ Zip________

Company Name________

PLEASE CHECK ACCOMMODATIONS FOR COMPCON 72

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<th>Type of Accommodation</th>
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<th>DELUXE</th>
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<tr>
<td>Single (1 person)</td>
<td>$20-$22</td>
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<tr>
<td>Double Bed (2 persons)</td>
<td>$24-$25</td>
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<td>Twin</td>
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<td>Studio Twin</td>
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<td>Large Two Room Suites</td>
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Luxurious International Suites:
(2 Rooms) □ $82 (3 Rooms) □ $106

PLEASE NOTE: RESERVATIONS MUST BE RECEIVED TWO WEEKS PRIOR TO COMPCON 72 IN ORDER TO BE CONFIRMED.
*Rooms will be held until 6 p.m. on day of arrival unless accompanied by deposit to cover first night's rental. Extra beds in any of above rooms, $5.00 each.
A one-day tutorial on semiconductor memories, sponsored by the College of Engineering, UC Berkeley, and the IEEE Computer Society, will be held Friday, September 15, at the Jack Tar Hotel. This one-day tutorial will cover the following semiconductor memory topics from the user's viewpoint:

BIPOLAR AND MOS CIRCUIT DESIGN — read-write, read-only, shift register; decoding, interfacing, power gating; static and dynamic techniques; and speed-power trade-offs.

PACKAGING, INTERCONNECTION, AND ECONOMICS — dual inline, beam leads, flip chips; yields, costs and trends.

RELIABILITY AND MAINTAINABILITY — failure modes; error detection and correction; system-level strategies.

MEMORY SYSTEM EXAMPLES — IBM System 370 Model 145; dynamic MOS systems; shift register systems.

CONCLUSIONS AND PROJECTIONS — performance and power limits; impact on digital system organization; market considerations.

The lecturer is David A. Hodges, Associate Professor of Electrical Engineering and Computer Sciences, University of California, Berkeley, and a consultant to both Signetics Corporation and Vidar Corp. Professor Hodges received his B.E.E. from Cornell University and M.S. and Ph.D. degrees from Berkeley. From 1966 to 1970 he was at Bell Laboratories, serving finally as head of the System Elements Research Department.