R-71-130. Gowdy, J. N., and Brubaker, T. A. Register Length Requirements to Prevent Overflow in Fixed Point Digital Filters. (6 pp.; Colorado State University, Fort Collins, Colo.)

A derivation is given for the register length that is necessary and sufficient to prevent overflow in a general nth order fixed point digital filter implemented using two's complement arithmetic. Results are valid for both the direct and canonic form.


The problem of realizing a fundamental mode asynchronous sequential circuit is considered. The presence of a pulse at the input of any memory element in the circuit may lead to pulse mode operation, even when all the inputs to the circuits are levels. It is shown that every fundamental mode asynchronous, single input change restricted flow table, is realizable by a pulse mode asynchronous sequential circuit. It is also shown that any fundamental mode asynchronous definite flow table is realizable by a feedback-free circuit of gates, delays, and S-R flip-flops. The shift registers constructed with S-R flip-flops are identical to those used in the synchronous case.


The discrete Fourier transform (DFT) of a sequence of N (non-prime) data points can be computed very efficiently by means of an algorithm called fast Fourier transform (FFT) described by Cooley and Tukey in 1965. Cooley and Tukey also proved that the use of a factor 3 in decomposing N is generally the most efficient. Glassman proved that this algorithm can be programmed in such a way that its efficiency is greatest for the factor 2. It is also known that in the special cases N=2^m or N=4^m the algorithm may be programmed in a special way that makes the efficiency still greater. This paper describes a computer program based upon an algorithm which has been selected in such a way, that the general case (N=R^1R^2...R ) as well as the special cases N=2^m and N=4^m are treated in the most efficient way.

R-71-133. Pohl, I. A Sorting Problem and Its Complexity. (11 pp.; University of California, Santa Cruz, Calif.)

A technique for proving min-max norms of sorting algorithms is given. One new algorithm for finding the minimum and maximum elements of a set with fewest comparisons is proved optimal with this technique.


The computers constructed by the School of Electrical Engineering of the University of Sydney are listed, and the hierarchical (two-level) computer control system under development is described. The interrupt structure for the higher level computer which provides priority arbitration over both cycle stealing and program change requests is detailed. This is used for the interfacing of peripherals (e.g. a disk) and for the communication with the lower level computer. Major features of the system which are considered desirable for real-time multi-user systems are then described. An example is the unique hardware multi-level core protection facility in the higher level computer. Finally the organization of the high-speed computer-to-computer communication system utilizing an asynchronous databus is presented.
R-71-135. Hight, S. L. Complex Disjunctive Decomposition of Incompletely Specified Boolean Functions. (35 pp.; Bell Laboratories, Denver, Colo.)

In this paper, the Ashenhurst-Curtis theory of complex disjunctive decompositions is extended to the realm of incompletely specified Boolean functions. A compatibility relation on the columns of the decomposition chart is introduced which is applied to identify all possible simple disjunctive decompositions for each input partition. The assignments of the don't-care (d) conditions which are required to realize these simple decompositions are described by a vector listing the constraints on these d's by new Boolean variables called constrained don't-cares. A compatibility relation is introduced on these vectors, called constrained Boolean vectors, which is applied to form complete decompositions. A complete decomposition is one for which all possible simple decompositions have been combined into a complete decomposition.

Throughout the procedure, the freedom of choice implied by the d's is maintained as far as is allowed by the choices which have been made to achieve the decompositions.

R-71-136. Santos, E. S. First and Second Covering Problems of Quasi Stochastic Systems. (23 pp.; Youngstown State University, Youngstown, Oh.)

The first and second covering problems of stochastic sequential machines (SSM) have been investigated by Ott and Paz, respectively. In order to obtain more insights to these problems, quasi stochastic systems (QSS) are considered in this paper. Although finite-state systems similar to QSS have been introduced by other authors, they have never been studied systematically.


A method of solving covering-closure tables by an expansion of the underlying Boolean function is presented. The method is computer oriented and is computationally feasible for tables up to 25-30 rows. All solutions for a given cost criterion are generated.

R-71-138. O'Keefe, K. H. Modularity in Design: Shift Registers and Counters Used as System Building Blocks. (20 pp.; University of Washington, Seattle, Wn.)

An algorithm for determining whether or not an arbitrary sequential machine can be synthesized using only shift-registers or up-down counters as memory elements is presented. When realization is possible, a basis for state assignment is given. State-partitioning techniques are used to this end and it is concluded that by means of a single test, it is possible to simultaneously check for realizability using either of the two module types. Thus, a significant step is made in the development of a unified theory for modular synthesis of sequential machines. Examples are presented.

R-71-139. Ippolito, J. C. Synthesis of Switching Functions in Cellular Networks. (15 pp.; Laboratoire d'Automatique, Toulouse, France.)

The development of microelectronic techniques, and particularly of mean and large scale integrated circuits has motivated, since 1960, numerous studies on certain types of switching structures, called cellular or homogeneous networks. These networks involve three main types of problems:

• choice of a basic cell of moderate complexity
• design of system synthesis methods
• minimization of network dimensions and of the number of external connections.

This paper deals with this type of cellular network and offers a particular approach to solve the above problems.

R-71-140. Azema, P. Decomposition of Switching Functions Into Linearly Separable Switching Functions. (19 pp.; Laboratoire d'Automatique, Toulouse, France.)

This paper deals with a particular method of decomposition of any switching function into linearly-separable switching functions or threshold switching functions. The procedures presented are based on the notions of optimal realization and boundary matrix of threshold functions. These procedures lead to the two following types of decomposition:

\[ F = G_1 G_2 \cdots G_p \] \[ F = F_1 F_2 F_3 \cdots F_2 F_q = F_{2q-1} \]

where \( F \) represents any switching function of \( n \) binary variables, and the functions \( G_i \) and \( F_i \) are all threshold switching functions of \( n \) variables.

R-71-141. Fuller, S. H. An Optimal Drum Scheduling Algorithm. (65 pp.; Stanford University, Stanford, Cal.)

Suppose we have a set of \( N \) records which must be read or written from a drum, fixed-head disk, or similar storage unit of a computing system. The records are of varying length and arbitrarily located on the surface of the drum. An algorithm is developed which will schedule the processing of these records so as to minimize the total amount of rotational latency (access time), taking into account the current position of the drum. This algorithm has the attractive property of exhibiting a computational complexity on the order of \( N \log N \). The general approach taken by the algorithm is to consider the schedule for processing the records as a single cycle permutation over the set of records. It first finds a permutation that minimizes the total latency time, regardless of the number of disjoint cycles in the digraph representation. This algorithm then transforms the minimal latency time permutation into a single cycle permutation while increasing the latency time of the schedule as little as possible.


If a linear continuous system is to be simulated — as it often happens — on a digital computer, then the behavior of the system is approximated by a set of difference equations. If the systems are described by their transfer functions, then the question arises as to which discrete transfer function should be assigned to a given continuous transfer function. A number of methods have been proposed for doing this (such as the impulse invariance method, the bilinear transformation, Boxer and Thaler's method and others).

In the case of real-time simulation the approximation algorithm has to lead to a so called "open" difference equation, which means that the current input value cannot be used to compute the output value occurring at the same instant of time. Most proposed methods — as the ones mentioned above — generally do not lead to open difference equations. It has been shown that the impulse invariance method — if normalized properly — is the optimal method as long as the input signal is bandlimited to the Nyquist frequency. If this is not the case, an alternative method is proposed to this paper attempts to present an optimal method in the above mentioned sense with the additional conditions that the resulting difference equations be always "open" and that it does not require special modeling of the system to be simulated such as normalization or other optimization procedures thus making automatic system modeling or adjustment possible.

R-71-143. Larson, A. L. A Decoding Iterative Array for Multiplication of Two's Complement Numbers. (10 pp.; University of Wisconsin, Madison, Wis.)

An iterative array for multiplication of signed binary numbers in two's complement form is presented. Through the use of a recoded algorithm, the number of cells is reduced significantly from the number used in earlier arrays.

R-71-144. Parrish, E. A. Suboptimal Solution of Large Multiple Output Prime Implicant Charts. (17 pp.; University of Virginia, Charlottesville, Va.)

This paper presents a reduction technique for finding (in general) suboptimal solutions to the covering problem of multiple output switching circuits. The technique is based on an algorithm for finding (in general) suboptimal solutions to the covering problem of single output switching circuits. An example is presented to illustrate the method.


It is well known that there is possibly a tradeoff in the binary representation of floating-point numbers in which one bit of accuracy can be gained at the expense of halving the exponent range, and vice versa. This paper suggests a way in which the exponent range can be greatly increased while preserving full accuracy for most computations.


A class of faults called primary input faults is defined. Necessary and sufficient conditions on a combinational switching function f to be realizable as a combinational net N tolerating primary input faults are developed. An m-fault-tolerant combinational circuit is defined. Then it is shown that combinational net designed for tolerating m primary input faults will be m-fault-tolerant. Two different procedures for realizing a switching function by m-fault-tolerant combinational net for any desired m is given. Relative merits of these two procedures are studied. An m-fault-tolerant sequential machine is defined. Realization of an m-fault tolerant sequential machine is shown. Two modes of fault tolerance are defined as random and burst fault tolerance. Burst fault tolerance of the m-fault-tolerant machine is studied. A hazard mode is defined as k-static-hazards. The relation between hazard free realizations and m-fault-tolerant realizations is shown.

R-71-147. Mitran, I. Approximation of Turing Machines. (5 pp.; University of Newcastle upon Tyne, Newcastle upon Tyne, England.)

An attempt is made to define the notion of "distance" between the computations of Turing Machines. The problem of approximating a Turing Machine is considered and theorems about the possibility of such approximation and about the kind of possible approximation are proved. The notion of distance is then defined for languages and the implications briefly explored.
A direct method of determining the maximum compatibility sets of an incompletely specified flow-table of a sequential machine is presented. Subsets of pairwise incompatible are utilized to decompose the set of all states in a step by step process into the maximum compatibles in a few steps. The method is simpler and faster than previously reported tabular, algebraic and graphical techniques.


A model is described for use in the realization of solutions for serial processing problems of the type common to pattern recognition and coding tasks. In particular, the model is applicable to any decision type task where an output is required only upon the receipt of the final symbol of a fixed length input string. It is shown that state minimal solutions for such tasks may be generated as final output sequential processor by a direct tabular technique.

R-71-150. Reddy, S. M. A Design Procedure for Fault Locatable Switching Circuits. (23 pp.; University of Iowa, Iowa City, Iowa)

A technique to design fault locatable combinational switching circuits is given. The networks resulting from the application of the proposed technique have at the utmost four levels of gates.


A proof is given of a method proposed by Lackey and Melzter for determining the selection of Rademacher functions which must be combined to generate a specified Walsh function. The method provides a convenient way of digitally controlling a Walsh function generator.

R-71-152. Huang, J. C. An Algebraic Model for Data-Base Management Systems. (39 pp.; University of Houston, Houston, Tex.)

Presented in this paper is an algebraic model for the information processing systems generally known as data-base management systems or fact retrieval systems. Essentially, this model is an algebraic system in which information storage and retrieval operations are formalized as the composite functions of four functions, each of these accounts for information structure, search strategy, memory allocation, and relevancy between queries and information items. As a result, we have devised two algorithms that can be used as the theoretical tools for creating optimal information structure for specific applications. The model will not only be useful for analysis and synthesis of data-base management systems, but also provide us with a basis for developing a unified algebraic theory on the subject. The model also provides us with a framework in which one can easily embed problems in information retrieval into problems in the theory of finite automata. For example, it is established that the design of an information structure (or file structure) corresponds to the construction of a labeled directed graph or an algebraic system, which can be construed as a generalized finite-state sequential machine. Hence the process of memory allocation is analogous to state assignment in the theory of sequential machines.

R-71-153. Ehrich, H. D. A Note on State Minimization of a Special Class of Incomplete Sequential Machines. (7 pp.; Technischen Universitat Hannover, Hannover, West Germany.)

In this note a necessary and sufficient condition is supplied for a flow table to have the property that every cover composed of maximal compatibles is closed. An example of such a flow table is given to which all sufficient conditions known before do not apply.


Many cases arise in practice where a versatile hardwire pseudorandom number or pseudonoise generator would be extremely useful. General purpose pseudonoise devices are not available today. We present a new sampling method, conditional bit sampling, which is suited for hardwire sampling devices because of its generality, simplicity and accuracy. Random variables sampled from an arbitrary distribution are generated bit by bit from high- to low-order bits with the conditional bit algorithm. The result of a comparison of a uniform number to a conditional probability determines whether a bit in the sampled random number is set to one. The conditional probabilities are easily calculated for any probability distribution and must be arranged in special order. Simple FORTRAN programs make all necessary computations. Agreement between actual and theoretical performance of the conditional bit-algorithm was excellent when sampling accuracy was evaluated for several examples of continuous and discrete densities. Sampling from empirically known, perhaps erratic-shaped, densities presents no problems. Only a small memory containing the conditional probabilities needs to be changed to alter the sampled distribution. The conditional bit arithmetic process always remains the same.


A hardwire device which produces a voltage with arbitrary amplitude distribution was constructed using a "conditional bit" algorithm to sample from an arbitrary voltage amplitude distribution. The sampling algorithm and hardware processor are independent of the distribution sampled. Only a small read-only memory needs to be changed to alter the distribution sampled. It is possible to compute the accuracy of the sampled random variables from knowledge of read-only memory contents. The sampling accuracy of the device may be arbitrarily increased by varying any of several design parameters. Our particular pseudonoise generator produced 200,000 random seven bit variables per second. Contents of read-only memories for both Gaussian and an arbitrary density were computed so that the maximum error was less than 2.73% (average error 1.0%). The output voltage accuracy was better than 1%. Both the sampling speed and accuracy of a conditional bit pseudonoise generator can be increased much in excess of our implementation.