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The progress of large scale integration (LSI) has increased the difficulty of testing and diagnosis. The automatic test pattern generation method for the single stuck type of fault for combinational circuits is considered in this paper, based on Boolean difference theory. Boolean difference is previously defined and programmed as a mathematical tool for analyzing logic circuit errors and designing error detecting circuits, although some exposure on using it for test pattern generation has been given. This paper discusses basic theories and a programming implementation of an algorithm for combinational circuits. Results of examples run on computers show that the Boolean difference technique gives maximum fault coverage on combinational circuits and from very good to maximum fault coverage on asynchronous sequential circuits. The program language is currently written in FORTRAN. The technique of using Boolean difference allows test pattern generation procedures to be systematic and clear to understand. The result is an equation-solving procedure rather than an exhaustive tabular approach.

R-71-93. Miller, G. and Jordan, B. W. File Operations In a Streaming Processor. (20 pp.; Bell Telephone Laboratories, Naperville, Ill.; Northwestern University, Evanston, Ill.)
This paper discusses computer organizations for nonarithmetic problems such as the file operations of sorting, searching, merging, and table look-up. The file operations considered here are on fixed length fields and records and are characterized by their repetitious treatment of such fields. Present computer organizations generally require several instructions imbedded in a loop to process two source operands. This loop is repeatedly executed for each operand pair to be processed, which creates overhead in terms of the relatively large number of machine cycles required to process long sequences of data pairs. Proposed here is a quiescent instruction format and register configuration which is included in a system (called a streaming processor) and which is capable of processing long data streams with considerably less instruction fetching and decoding. This approach results in a saving of machine cycles. Several file operations problems were simulated and compared with the same file programs executed by the IBM 360/65 computer.

R-71-94. Zahn, C., and Roskies, R. Fourier Descriptors for Two-Dimensional Shapes. (50 pp.; Stanford Linear Accelerator Center, Stanford, Calif.; Yale University, New Haven, Conn.)
A method for the analysis and synthesis of closed curves in the plane is developed using the Fourier Descriptors of Cosgriff. A curve is represented parametrically as a function of arc length by the accumulated change in direction of the curve since the starting point. This function is expanded in a Fourier Series and the coefficients are arranged in the amplitude/phase-angle form. It is shown that the amplitudes are pure form-invariants as well as are certain simple functions of phase-angles. Rotational and axial symmetry are related directly to simple properties of the Fourier Descriptors. An analysis of shape similarity or symmetry can be based on these relationships; also closed symmetric curves can be synthesized from almost arbitrary Fourier Descriptors. It is established that the Fourier Series expansion is optimal and unique with respect to obtaining coefficients insensitive to starting point. Several examples are provided to indicate the usefulness of Fourier Descriptors as features for shape discrimination and a number of interesting symmetric curves are generated by computer and plotted out.

This paper describes a set of register transfer modules (called RTMs) which are used as a basis for digital systems design. RTMs have the property of allowing a digital system to be specified in a register transfer flow chart form which has complete construction (wire) information, thus avoiding the usual combinatorial and sequential switching circuit design. The paper first describes the digital systems design problem (i.e., what digital systems engineers do) as the definition of the problem for which RTMs may be the solution. We then present the basic decisions made in the design of the modules. The complete set of RTMs are described, from the user’s viewpoint. Four examples of actual digital systems designs provide the reader with an understanding of their use. We intend to present sufficient detail within the paper to allow a reader to understand and use RTMs to solve digital systems design problems.

R-71-96. Stoffers, K. E. Determination of Maximum Compatible. (28 pp.; Sacramento State College, Sacramento, Calif.)
The relation “compatibility” is symmetric and reflexive; in contrast to “equivalence” it is not transitive. Maximum compatibles (maximal classes of elements which are all pairwise compatible) are not mutually exclusive and can partially overlap each other. Maximum compatibles can be visualized as the
maximal complete subgraphs of a symmetric graph. The paper describes the following approaches to the finding of maximum compatibles:

a. Merging and splitting of sets based on compatible and incompatible pairs respectively.

b. Use of switching algebra in connection with incompatible pairs.

c. An algorithm which uses Boolean operations between rows of the compatibility matrix.

The discussion pays particular attention to the relative merits of the various techniques for the solution of large problems. The material presented under (a) and (b) has originated with others. The algorithm (c) is the author's own development.

R-71-97. Gilman, I. An Algorithm for Nonsupervised Pattern Classification Using Stochastic Approximation. (88 pp.; Bell-Northern Research Ltd., Ottawa, Canada.)

An algorithm for the classification of a data set into an initially unknown number of categories is presented. This algorithm is an improved version of a previous one, achieved by replacing the latter's mode estimation procedure by one which uses a stochastic approximation technique. The algorithm has been used in experiments with multi-category artificially generated data sets; and compared with an optimal recognition scheme.

R-71-98. Parchman, R. The Number of State Assignments for Sequential Automata. (4 pp.; Mathematics Institute, Hanover, West Germany.)

In a new theorem proved by elementary combinatorial results, the number of nonequivalent state assignments is determined. The number of nondegenerate state assignments is also computed.


When two or more processors attempt to simultaneously use a functional unit (memory, multiplier, etc.), an arbiter module must be employed to insure that processor requests are honored in sequence. The design of asynchronous arbiters is complicated because multiple input changes are allowed, and because inputs may change even if the circuit is not in a stable state. A practical arbiter and its implementation are presented. Implementation of various priority rules (linear, ring, mixed) is discussed, and building large arbiters with trees of two-user arbiters is considered.

R-71-100. Friedmann, P. G. Comment on "Optimal Curve Fitting with Piecewise Linear Functions." (8 pp.; Leeds & Northrup Co., North Wales, Pa.)

A simple iterative technique is presented for constructing a piecewise linear approximation that minimizes maximum absolute error. The function \( y(x) = 100 \sin(x) \) is approximated over the range \( 0 < x < \pi / 2 \) with maximum absolute error almost 30% smaller than that achieved by Cantoni in the subject paper.

R-71-100. Friedmann, P. G. Comment on "Optimal Curve Fitting with Piecewise Linear Functions." (8 pp.; Leeds & Northrup Co., North Wales, Pa.)

oratories, Holmdel, N.J.)

An algorithm is described which generates the set of representative functions of the NPN (negation and/or permutation of variables and negation of the functions) classes of state Boolean functions. The set is based upon integer programming techniques. The set of representative functions for the NPN equivalence classes of unate functions of 6 or fewer variables were obtained using this algorithm.

R-71-102. Desai, B. C., and Marin, M. A. Ordering of Implicants in a K-Element Boolean Algebra. (22 pp.; Loyola College, Montreal, Canada; McGill University, Montreal, Canada.)

The set of conjunctions disjunctions and negation of k valued discrete variables and their functional relationship may be represented by a set Y of equations (conditions) derived from the word description of a problem under consideration. The validity or non validity of Y as a function of the state of the independent variable is of importance. An ordering of the set of implicants of Y is investigated in this paper and an algorithm for parallel processing of terms is proposed. The proposed algorithm is suitable for hardware logic realization and thus may be designed as an independent parallel processor within the CPU of a general purpose computer.

R-71-103. Matheson, W. S. Switching Circuit Design, Using Information Theory. (22 pp.; University of Essex, Essex, United Kingdom.)

A switching circuit design philosophy is presented which uses the idea that some information embedded in the input information is required to be passed by the switching circuit to the output. The remaining information is to be blocked. The amounts of information concerned can be quantified by assuming a probability distribution for the input signals. A simple algorithm is presented which builds up a realization for a switching function from input to output, by looking for interconnections of gates that produce functions which are "relevant," in the information sense, to the desired output function. It is found, at least for small numbers of input variables, that "good" realizations are generated rapidly. Advantages of this approach are that topological constraints can be built into the algorithm without changing the basic procedure, and that the algorithm is easily programmable. Extensions of the algorithm to cover 2-dimensional array realizations and multiple-output functions are discussed.


The paper presents a new algorithm \( A^* \) for the synthesis of minimum gate bit TANT networks. This algorithm, which differs in the setting up of the CC Table from the known Gimpel algorithm, displays very advantageous features, both in its manual as well as computer realization. The final stage of this synthesis is the solution of CC Table. The second problem discussed in the paper is the synthesis of minimal logical networks having no static hazards. The McCluskey table has been extended and modified, and an algorithm for the synthesis of minimal, hazardless two-level AND/OR networks has been proposed. This algorithm has been adapted for the synthesis of minimal, hazardless TANT networks, in result of which its simplified version, \( A_b \), has been obtained. Both \( A^* \) and \( A_b \) algorithms are suitable for manual realization in the case of functions having as many as 6 variables. For functions with a greater number of variables a computer program has been worked out.

R-71-105. Clegg, F. W. The SPOOF: A New Technique for Analyzing the Effects of Faults on Logic Networks. (42 pp.; Stanford University, Stanford, Calif.)

In general, one cannot predict the effects of possible failures on the functional characteristics of a logic network without knowledge of the structure of that network. The SPOOF or structural pattern of failure function described in this report provides a new and convenient means of characterizing both network structure and output fault in a single algebraic expression. A straight-forward method for the determination of a SPOOF for any logic network is demonstrated. Similarities between SPOOF's and other means of characterizing network structure are discussed. Examples are present which illustrate the ease with which the effects of any "stuck-at" fault — single or multiple — on the functional characteristics of a logic network are determined using SPOOF's.

R-71-106. Clegg, F. W., and McCluskey, E. J. Algebraic Properties of Faults in Logic Networks. (145 pp.; Stanford University, Stanford, Calif.) (Price: microfiche $4.50; photocopy $9.00)

This work describes a general study of the effects of so-called "stuck-at" faults on the structural and functional characteristics of combinatorial logic networks. It is shown that some of the possible faults which can occur in a given network bear relations to certain other possible faults in that network. Knowledge of these relations greatly facilitates investigation of networks in the presence of failures. The two types of relations considered are those of covering and equivalence. The covering relations introduced reflect the mechanisms whereby the presence of certain faults in a network renders the occurrence of other failures to some extent unobservable. The equivalence relations which are presented reflect the varying degrees to which distinct faults in a network can be indistinguishable. Some of the applications of the knowledge obtained by these techniques of the properties of, and relations between, faults is described. In particular, it is shown that knowledge of the relations between faults has important and immediate usefulness in the area of failure detection and diagnosis.


Dynamic memories are commonly constructed as circulating shift registers, and thus have access times that are proportional to the size of memory. When each word in a dynamic memory is connected to r words, r \( \geq 2 \), access time can be proportional to the base r logarithm of the size of memory. This paper describes a memory that achieves minimum access time for \( r = 2 \). The memory can also be operated in an efficient binary search mode. Slight variations of the interconnection patterns lead to a memory that is well suited for FFT and certain matrix computations.

R-71-108. Carroll, J. D., Kruskal, J. B., and Wish, M. Multidimensional Scaling and Closely Related Topics: Selected, Annotated References to Papers, Programs, and Work in Progress. (8 pp. Bibliography; Bell Telephone Laboratories, Murray Hill, N.J.)

Within sections, published papers are listed chronologically. We regret any inadvertent omissions of papers which should be included. In forming this logic net listing, we have been greatly aided by the extensive bibliographies gathered by Paul Green and Frank Carmone. We hope to expand this listing, and perhaps bring it up to date, from time to time. The present list is current as of October, 1970.


The reduction of multi-variable logic functions has always been a problem. The Veitch diagram is useful for quick reduction of logic functions with up

The theoretical foundations of a FORTRAN-written program are described, which computes test-patterns for error detection or error diagnosis in combinational or sequential digital networks. The detection capability of the different classes of faults and the reaction of the algorithm on the logic error types are well known and presented in this paper. The mathematical tools to generate such test-patterns are the Boolean Differences of the logic networks.

R-71-111. Carroll, B. D. Minimum Two-Level Threshold Gate Realizations. (42 pp.; Auburn University, Auburn, Ala.)

This paper deals with the synthesis of two-level networks of threshold gate logic elements which realize non linearly separable switching functions with a minimum number of logic elements. An algorithm based on the tree procedure of Coates and Lewis is developed which can be used to obtain the desired network realization for a given switching function. The function may be incompletely specified. A non linearly separable switching function has properties referred to as inconsistencies which cause void ranges to occur in the tree realization procedure. These inconsistencies must be removed by the addition of gates to the network structure before a realization of the function can be obtained. The algorithm is based on determining when a set of inconsistencies can be removed by a fixed number of gates which realize linearly separable functions. Necessary and sufficient conditions for removing an inconsistency are developed. A Boolean function technique for applying the removal rules to a set of inconsistencies is given. This technique consists of defining a Boolean function called a constraint function for each inconsistency that has been encountered. The product of constraint functions indicates the unsatisfiability of defining gates to remove the inconsistencies. A zero product of constraint functions indicates that the set of inconsistencies cannot be removed with the number of gates being used.


In this paper we present algorithms for designing fault-detection experiments for sequential machines with special emphasis on the case in which the machine does not possess a distinguishing sequence. The length of an experiment is reduced through (1) identifying each state with its own unique input/output set rather than using a common set for all states, (2) utilizing overlapping of the required input/output sequences so that a portion of the experiment serves more than one purpose, and (3) verifying the reference condition in which the machine is placed at many points in the experiment by as short a locating sequence as possible. Important distinctions are made between locating sequences of the type introduced in previous work and those defined and used here.

R-71-113. Cerny, E., and Marin, M. Identification of Solutions in a System of Boolean Equations. (9 pp.; McGill University, Montreal, Canada.)

A method for solving generally related Boolean relations and the identification of their solutions with respect to each Boolean relation is presented.

R-71-114. Kamat, D. S., and Plite, M. V. A Computer Controlled Picture Scanning Device with Special Reference to Bubble Chamber Pictures. (70 pp.; Tata Institute, Bombay, India.)

(Price: microfiche $3.00; photocopy $6.00)

This report proposes an electronic-optical scanning measurement system which will be capable of measuring bubble chamber tracks with a resolution between 2-3 um on film in a direction orthogonal to the track. The intended resolution in the direction of the track will be 10 um on film. This is to be achieved by projecting a cathode ray beam spot on a film transparency, and by picking up the light beam on the other side of the film by a photo-multiplier. The movement of the beam spot is controlled by an on-line computer. The obscuration data is accumulated for a scan line length of 0.3 mm on film. After the completion of the accumulation of data on 128 scan lines, the on-line computer is made to compute the Walsh transform of the digitized pictures in real-time. It is shown that a considerable reduction in total time for the transformation of a picture results, if the process of scanning a picture overlaps with computations. This is accomplished by operating on each picture line as it is generated from the scanner, instead of starting the transformation operation after the entire picture has been scanned. Two theorems are presented which decompose a picture by row or by column to facilitate real-time transformation. For digital computer processing, such a decomposition reduces the storage requirements by a factor of two. Based on these theorems, a hardware machine is designed to perform parallel Walsh-Hadamard transformations.


In an associative cache memory system the least-recently-used algorithm may be used to determine which data should be purged to free memory. Some of the known solutions to the postage stamp problem can be used to optimise speed of operation in the face of constraints on serial gate delays and fan-out.


The paper contains the solution of the problem of the existence of an analogue with periodic-variable structure of a given, fixed-structure, connected automaton. Using a Boolean approach, we prove a necessary and sufficient condition for the existence of the periodic analogue and we give also an algorithm which enables us to find actually this analogue. The saving of the memory capacity needed for the construction of a given automaton is the main interest of the existence of a periodic analogue.


The definition of the generalized fault table is expanded to cover a representation employing more than one fault cube per fault pattern. On the basis of this expanded definition and simple concepts from a cover algebra, new procedures are developed for finding first and second order diagnostic resolutions.


The adequate representation of a given set of data can often be achieved with a number of clustering techniques. Further analysis of interrelationships among identified clusters is a necessity in many classification problems. This study describes an approach to the analysis of relationships between clusters. This approach utilizes geometrical relations among pertinent cluster mean-vectors in pattern space. The described analysis is applicable to both binary and continuous data, with any number of dimensions. A speech recognition problem with 200-dimensional, binary data, clustered by the Frischfeld and Fiscer clustering technique is used to illustrate the proposed algorithm. The information about the distribution of these speech data obtained through the application of the algorithm may be helpful for further research in the area of speech recognition. The algorithm should be of special importance for those classification problems in which each class of given patterns can be represented by more than one cluster or mode.


The concept of Boolean difference has been used to examine various properties of Boolean functions and to derive test-input vectors for detecting faults in combinational logic networks. This paper introduces the notion of time-dependent Boolean difference which extends the Boolean difference concept to digital networks endowed with memory properties. In defining the time-dependent Boolean difference, no restrictive assumptions are made; and as formulated in this paper it is equally applicable to both fundamental-mode and pulse-mode systems.
R-71-121. Kermani, Mehdi B. Projection, Angle Clustering for File Structure and Retrieval. (10 pp.; Arya-Mehr University, Tehran, Iran.)

The problem of file structure and information retrieval is a subject of vital interest to government and businesses. It is here attempted to review and introduce a new method of file organization by which a fast access to the items of the file becomes possible. It is shown that the entire document file may easily be decomposed into its constituents to better satisfy the request and this new decomposition results in the file query answers.

R-71-122. O'Keeffe, Kenneth H. Residue Arithmetic with Improved Scaling and Sign Detection. (19 pp.; University of Washington, Seattle, Wash.)

A special class of residue number systems which have only odd moduli of the form $2^n-1, 2^n-2, \ldots, 2^n-k$, is considered. Emphasis is placed upon the problem of finding practical methods of "scaling down" and sign detection in such systems. A residue system evolves in which efficient methods are demonstrated, for the case of $k=2$, for mechanizing the operations of addition, subtraction, general multiplication, multiplication by 2, division (with truncation) by 2 and sign detection. The resultant system can operate faster than either conventional weighted systems or many-modulus residue systems of equal complexity in applications involving division by 2 and sign detection.

R-71-123. Sintonen, L. On the Realization of Functions in N-Valued Logic. (17 pp.; Tampere University of Technology, Tampere, Finland.)

This paper describes a system of N-valued logic which is based on a set of three basic functions. These functions are selected so that they are easy to realize physically with conventional electronic circuitry. Furthermore, the system is functionally complete.


An artificial touch perception system has been realized in order to study a method of processing information obtainable through tactile exploration of three-dimensional forms. The results can be useful for many purposes. The first part of the work concerns the project and realization of the tactile explorer. For this purpose we used some kind of artificial limb like a finger with a certain number of touch sensitive transducers distributed along the surface of the finger tip. The information received by touching the object with the finger is successively utilized as the input of the control servosystem which moves the finger point-by-point along the object surface, in order to proceed with the exploration of the examined object. The second part describes the use of the propositional calculus in logical classification of the objects, as a method of 3-D pattern recognition. Elaboration of the input data (obtained by tactile exploration) and computation of characteristic geometrical features of 3-D forms has been performed on computer.


A deductive method of fault simulation is described, which "deduces" the faults detected by a test at the same time that it simulates explicitly only the good behavior of a logic circuit. It appears to be significantly faster than "parallel" fault simulators, particularly for large circuits, but uses much more computer memory than do parallel simulators. The simulator is table driven, employs selective trace, models the dynamic behavior of circuits reasonably well but does not perform race analysis, and accommodates both synchronous and asynchronous circuits. It simulates three logic states: 0, 1 and "don't know." Results for a few logic circuits are given, obtained with a version of the simulator implemented on a Honeywell 635 computer. Versions exist for an IBM 360/67 also, and newer versions are under development.

R-71-126. Das, S. R. On Systematization of Finding All the Modified Cut-sets in an Incomparability Graph for Deriving Maximum Compatibility Sets. (26 pp.; University of Ottawa, Ottawa, Canada.)

A method for deriving all the maximum compatibility sets using the incomparability graph corresponding to a given flow table is recently proposed by Das and Sheng. The method is simple and complete, and derives the maximum compatibility sets by way of finding all the modified cut-sets of the incomparability graph. In the present study, in an attempt to simplify the process of generating the maximum compatibility sets, an approach is made to systematize the method of finding all the modified cut-sets in the incomparability graph corresponding to a given flow table.

R-71-127. Rasek, E. Translation Invariant Registration of Characters by Digital Computers. (52 pp.; Siemens AG, Munich, Germany.)

The capability of invariant registration of written or printed characters is a necessary prerequisite in technical reading machines to achieving high processing speed and simple hardware realization. The general principles of translation invariant registration and the method of finding them are given as well as the general ideas and conditions underlying our character-recognition system. Systematization and discussion of the methods of preregistration and translation invariant measurements build the mainframe of the paper. Features of their general usefulness and processing speeds on a Siemens 4004/45 are indicated.


This article describes a new heuristic programming approach to the problem of simplifying Boolean expressions. The method described considers a prime implicant-canonical term matrix developed directly from a Boolean function. Although the heuristic to be described is applicable to reduced matrices, due to the simplicity and speed of the algorithm an optimal or near optimal solution using the original matrix may be achieved in less time than would be needed to reduce the matrix using elimination methods. The matrix is assumed to have equal weights assigned to prime implicants and the minimization criterion is the coverage of all canonical terms with the fewest number of prime implicants. The algorithm is suitable for hand calculation of medium size (a 2500 term prime implicant-canonical term matrix) problems or computer solutions to large scale (prime implicant-canonical term matrices of over 700,000 elements) problems. Results of the algorithm for a large number of sample problems are given.

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