
Optimal networks consisting of NOR-OR gates (each gate produces the NOR and/or the OR of its inputs) are tabulated for all Boolean functions of three variables. Optimality is defined as minimizing first the number of gates and then the number of interconnections. The optimal networks were synthesized for each Boolean function by using an integer programming synthesis technique.


The bandwidth limitations of the practical analog computer units lead to dynamic errors in the computer solution. In this correspondence the authors report a unified approach to represent these errors, generalized for a system of simultaneous linear differential equations with constant coefficients. It is also shown that these errors can be compensated by setting the system after initial perturbations in its constant coefficients as well as its driving functions.


Given some unknown object, belonging to a known finite set of n possibilities, it is required to determine its identity by successive comparisons with each of the possibilities. Associating with each of these possibilities a testing cost and a probability that it is identical to the unknown object, we would like to obtain such a testing procedure which has minimum expected testing cost. Intuitively, it would appear that one should proceed by always applying the remaining test with least cost/probability ratio. We show that this technique does not necessarily yield the optimal procedure and present an algorithm which determines the optimal testing sequence in a number of steps proportional to n\log_2 n. Applications to fault location and computer programming are described.

R-71-69. Wynn, A. C. Parity Function Theorems. (9 pp.; Arizona State University, Tempe, Arizona.)

This article presents special theorems which greatly simplify the process of determining whether a given Boolean function is an odd or an even parity function. The logic operations utilized for these theorems are the Exclusive-or and Coincidence operators. The theorems are restricted to the use of these two Boolean operators.


A method is introduced for deciding the class of a pattern described by a
vector of measured features. Memory requirements and the time required for classifying a pattern are not excessive even when there are many classes and many multilevel feature measurements. First the number of classes considered possible for a pattern to be classified is drastically reduced by eliminating each class every training sample of which is far from the pattern by a rough measure of distance. Then additional tests decide among the few classes that remain possible. The first step is facilitated by prereduced histograms of the features of the training patterns. The additional tests are refined to classify the same training patterns correctly. The method is tested experimentally. A network of about 30000 algorithms of algebraic operations and weights. The characters range widely in quality. One third are taken as training patterns and the rest used to test the method. The features used are the characteristic loci.


This paper reports experiments in which the recognition of Highleyman's handprinted numerals was a few per cent more accurate when numerals and letters were used as a training set than when only numerals were used as a training set. The inner loop iteration was emphasized, and both software and microprogramming techniques are presented for achieving speed-ups. A hardware facility is then described for improving highly iterated loops containing Boolean decisions.

R-71-73. MacDougal, M. H. A Note on the Interruption of Extended Core Storage Transfers. (11 pp.; Control Data Corporation, Palo Alto, California.)

In the Control Data 6000 system, transfers between central memory and extended core storage may be interrupted through the issue of an exchange jump by a peripheral processor. Reinitiation of the transfer requires that it be run as a test system rather than resumed at the point of interruption. The transfer process locks out the CPU, so an interrupted transfer results in lost CPU time. In this paper, an estimate of this time loss as a function of interrupt rate, transfer length, and transfer initiation overhead is obtained, as well as an estimate of the transfer length which minimizes lost CPU time.

R-71-74. De Morri, R., and Meo, A. R. Reduced Parallel Multipliers and Errors Involved. (15 pp.; Consiglio Nazionale delle Ricerche, Torino, Italy.)

The mean-square-error due to the elimination of a given number of columns in the elementary product matrix is calculated and compared with the "inherent" error due to the rounding-off of the factors. Such analysis shows that it is always possible to suppress many columns in that matrix without substantially increasing the errors involved in the multiplication. Beside, the introduction of a correcting bias by means of few constant digits permits to further reduce the mean-square-error or to suppress other columns without increasing the mean-square-error. The hardware reduction made possible by the elimination of a given number of columns is evaluated in terms of components saved in the conventional parallel implementation with full-adders. A useful set of demonstrators of transferable learning was achieved as in the case of independent recognition class if a function $X_N(X_1)$ has an extreme value, where $X_1$ is a reference member of the $N$-th class. Typically, $(X_N(X_1)$ is the Hamming distance between $X$ and $X_1$ and in this case the function $f(X_1)$ is itself independent of recognition class. If $f(X_1)$ is not Hamming distance, but it is instead a class independent function which depend from training sets, transfer is possible, because the class-independence of $f(X_1)$ may be leant from patterns belonging to one set of classes and used in the recognition of patterns belonging to a different set of classes.

R-71-75. Chiang, A. C. L., Reed, I. S., and Banes, A. V. Path Sensitization, Partial Boolean Difference and Automated Fault Diagnosis. (23 pp.; Macrodata Co., Chatsworth, California; University of Southern California, Los Angeles, California.)

This paper emphasizes a tool employed in automated fault diagnosis: path sensitization by partial Boolean difference analysis. Motivated by the analogy between a processor and a communication system, a model for fault detection of a logic net is outlined from the standpoint of information theory. The classical "path sensitizing" technique is made systematic using the partial Boolean difference. This technique is based on a new theorem on the partial Boolean difference. Finally, a programmable fault detection algorithm is presented along with an example.


The problem of parallel computation of local operations using five differently organized parallel processing machines (the SASD, SAPD, P4SADD, and PAPD computers) is investigated. It is shown that for a special class of local operations, called window operations, there is a trade-off between computation time and machine complexity. It is also shown that for the PAMD computer, the computation time increases as the degree of disorderliness of the local operation increases. In conclusion, in the designing of special-purpose parallel processing machines, we must take into consideration the degree of disorderliness of the operations to be performed.

R-71-77. Bubnok, V. Masking Method for Minimization of Switching Functions. (60 pp.; Albiswerk Zurich A. G., Zurich, Switzerland.)

The results of the minimization of switching functions sometimes include prime implicants of the zero order which do not have any neighbor in the set of given switching terms. As no minimization is possible a new approach to a further simplification is proposed. For this purpose the chess board principle is explained. When using the existing relations between the terms it is as a rule possible to find appropriate groups of switching terms which can be expressed by rather simple EXOR-Terms. In order to retrieve such groups of terms the masking method is applied. The same method is advantageous also in finding simple expressions for the groups of prime implicants of the first and higher orders. Combining the two procedures remarkable simplifications of the results can be achieved. The new approach is illustrated on typical problems.

R-71-78. Bubnok, V. Chess Board Method for a Simplified Realization of Switching Functions. (34 pp.; Albiswerk Zurich A. G., Zurich, Switzerland.)

A complete or restricted set of prime implicants can cover the terms of the switching function with a more or less large redundancy. In order to find an irredundant form from the set of prime implicants it is necessary to eliminate those prime implicants which cannot contribute effectively to the strict minimum sum. The criterion for the right choice of the prime implicants is their weight from the point of view of their cost, and their ability to cover a maximum number of switching terms. This criterion assures the simplicity of the switching circuit and helps to increase its reliability. Successively the prime implicants with the highest weight are chosen.

R-71-80. Chien, R. T., and Hong, S. J. Error Correction in High Speed Arithmetic. (23 pp.; University of Illinois, Urbana, Illinois.)

In high speed multipliers, multiplication is activated by processing a group of bits in parallel. As a result, any defects in circuitry produces possible errors in positions which are separated by fixed periods. A class of codes for the correction of such iterative error patterns resulting from a single fault is presented in this paper. A decoding algorithm together with a simple implementation scheme is also discussed.


These are programs, written in the FORMAG language, which employ the perturbation methods of Krylov, Bogoliubov, and Mitropolsky in the solution of certain differential equations. These programs are also described in the complete paper which is also available in the society repository. A. Rink and W. Streiffer, "Application of Digital Computers to Solve Analytically a Class of Second Order Nonlinear Ordinary Differential Equations," IEEE Computer Society Repository R-71-17.

R-71-82. Jarvis, R. A., and Patrick, E. A. Clustering Using a Similarity Measure Based on Shared Near Neighbors. (29 pp.; Purdue University, Lafayette, Indiana.)
A nonparametric clustering technique incorporating the concept of similarity based on the sharing of near neighbors is presented. In addition to being an essential, parallel approach, the computational elegance of the method is such that the scheme is applicable to a wide class of practical problems involving large sample size and high dimensionality. No attempt is made to show how a priori problem knowledge could be introduced into the procedure.

R-71-83. Basu, D. K. Row-Column-Wise Shifting in a Multidigit Bidirectional Shift Register. (7 pp.; Jadavpur University, Calcutta, India.)

A novel method of digit shifting in a bidirectional shift register is described which provides substantial saving of components in terms of gates. In this method only the bits occupying the 1-position of the R-4-2-1 code can shift in either direction of the same digit. A new circuit is shown to change places among themselves. Eight clock pulses are required to shift the bits through one digit position, but the number of clock pulse requirements are independent of the number of digits involved in the shifting process. However, this shortcoming of speed reduction can be overcome by providing a separate clock for this purpose which may be several times faster than the system clock. The drastic reduction in component count and cost of the new method over the conventional one has also been illustrated. These together with the reduction of interconnecting leads and power dissipation leads to the possibility of fabricating multi-digit bidirectional shift registers in monolithic integrated circuit packages.

R-71-84. Van Voorhis, D. C. An Improved Lower Bound for the Bose-Nelson Sorting Problem. (12 pp.; Stanford University, Stanford, California.)

In this paper we present a constructive proof that the minimum number of comparators required for an N-input sorting network is at least \[ \sum_{k=1}^{N} \log_2 N^k. \]

This lower bound represents a linear improvement over the information-theoretic bound of \( \log_2 N^N \).


A model is presented which may be used to explain the differences between observed and actual binary signals. The development parallels the "signal-plus-noise" model used for real variables. An example application of the model is presented which provides insight into experimentally observed behavior of sample data used to establish binary feature vectors for certain pattern recognition systems.

R-71-86. Das, S. R. A New Algorithm for Generating Prime Implicants. (4 pp.; University of Ottawa, Ottawa, Canada.)

In a recent paper, Stagli et al describe a new algorithm for the generation of all prime implicants of a Boolean function. The present paper makes some discussions on the paper, and comments on the basic idea that the authors utilize in the development of the algorithm.

R-71-87. Rao, V. V., and Nordstrom, A. W. Heuristic Minimization of AND-EXCLUSIVE OR Realization of Switching Functions. (17 pp.; University of Iowa, Iowa City, Iowa.)

Based on certain heuristics, a computer algorithm has been developed to minimize the AND-EXOR realization of a given switching function using both complemented and uncomplemented literals. Though no proof could be arrived at about the optimality of suboptimality of the procedure, computer results for the four variable case have been very encouraging, suggesting that similar procedures might lead to an optimum solution of this long standing problem.


A model of two-dimensional linear iterative circuits is defined in the form of matrix equations. From the matrix equations a two-dimensional characteristic function is defined. It is then proved that a matrix satisfies its two-dimensional characteristic function. This property is used to form a diagnostic matrix. Finally the diagnostic matrix is used in a minimization technique.

R-71-89. Gonzalez, R. C., and Tou, J. T. A Test for Separability with \( \Phi \) Discriminant Functions. (28 pp.; University of Tennessee, Knoxville, Tennessee; University of Florida, Gainesville, Florida.)

A test for separability with \( \Phi \) discriminant functions is presented. The procedure is first developed for linear separability and then extended to encompass the more general case of nonlinear separability by \( \Phi \) discriminant functions. The test has three principal advantages which are not shared by any algorithm previously developed: (1) A solution is guaranteed if the classes are separable, (2) the test is not an iterative procedure in the sense that it does not "converge" on the solution region, and (3) when the classes under consideration are not separable the test yields the best solution for a particular starting configuration.


This paper deals with the partial Boolean differences algorithm as used in fault diagnosis, and recommends a number of implementation strategies which may be desirable under certain conditions. Illustrations demonstrating the use of simple and higher-order partial Boolean differences are offered, and formulations relating the partial Boolean differences of a functional implementation to the conventional Boolean differences of the function are established.

R-71-91. Lazic, B. Z. On the Synthesis of Redundant Combinational Networks by Applying Majority Logic Decodable Cyclic Codes. (21 pp.; University of Belgrade, Belgrade, Yugoslavia.)

This paper discusses a method of synthesis of a redundant combinational multi-output network more reliable than a nonredundant (minimal) network. The proposed method uses a subclass of M (n,m) majority logic decodable, cyclic codes. The redundant network obtained in this way consists of an encoder part and of the corrector part. The encoder part is realized in the form of independent blocks (single-output networks). The output of the redundant network is error-free whenever the failures occur at most in two independent blocks of the encoder part (under assumption that a corrector part is absolutely reliable). The quantitative measure for the estimation of reliability improvement of the obtained redundant network over that of nonredundant network in the case when the corrector part cannot be taken as absolutely reliable is defined and the formulas for computing of this measure is given. Also, the way for estimating the cost increase of the redundant network over that of the nonredundant network is described. The main advantage of the proposed method is relatively low redundancy.