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R-70-196. Reed, I.S. Symbolic Design Techniques Applied to a Generalized Computer. (9 pp.; University of Southern California, Los Angeles, Calif.) Some techniques for the symbolic design of digital computers are developed and discussed. These techniques are then applied to the development of a generalized computer, having an internal nature that can be programmed with a sequence of micro-instruction. This machine has the capability of simulating the internal nature of any other computer that utilizes the same type of main memory. (This paper was delivered by invitation to an IRE-IEEE Computer Group Meeting at the Moore School, University of Pennsylvania in 1956. However, it was only recently submitted for publication.)

R-70-197. Pinter, Charles C. On Simplifying Truth Functions: A Preliminary Reduction of Coreless Formulas. (14 pp.; Bucknell University, Lewisburg, Pa.) The core of a truth function $\Phi$ consists of those prime implicates of $\Phi$ which are conjuncts of every conjunctive normal formula representing $\Phi$. The notion of a core is generalized here: a class of prime implicates of $\Phi$ is defined, called its "pseudo core." It is shown that the "pseudo core" is a part of each one of a class $I$ of normal forms of $\Phi$ where $I$ includes a simplest normal form. The "pseudo core" may be found easily and rapidly, plays the same role as the core in simplifying a formula, and may exist even in coreless formulas.

R-70-198. Larsen, Ronald W. and Reed, Irving S. Coding Versus Non-Coding Redundancy for Failure-Tolerant Sequential Circuits. (50 pp.; Naval Undersea Research and Development Center, Pasadena, Calif.) A synthesis procedure for failure-tolerant sequential circuits using error-correcting codes is presented. Coding and non-coding redundancy are then compared as to circuit complexity, cost, and reliability improvement. It is shown that for a specified error-correcting ability, non-coding redundancy yields better circuit reliability than coding redundancy at the expense of greater circuit complexity. When circuit complexity as well as reliability are taken into consideration, it is shown that schemes based on orthogonalizable codes provide a greater improvement in reliability for a given complexity than non-coding redundant schemes. As in any redundant scheme, these results presuppose reasonable good reliabilities for irredundant circuits.

R-70-199. Hoffner, Charles W., II, and Robinson, John P. Three-Level Realizations for Threshold Functions. (26 pp.; Bell Telephone Laboratories, Columbus, Ohio) This paper considers three-level AND-OR-gate realizations for threshold functions. The three-level realizations presented require substantially fewer gates and gate inputs than the minimum gate two-level realizations for the same functions. For example, the minimum gate two-level realization for the seven-or-more out of fourteen function requires 3,004 gates and 21,021 gate inputs; the three-level realization presented for this function requires 120 gates and 658 gate inputs.

R-70-200. Ibaraki, Toshio. Gate-Interconnection Minimization of Switching Networks Using Negative Gates. (36 pp.; Kyoto University, Kyoto, Japan) In this paper, we develop an algorithm to design a two-level switching network composed of negative gates with no fan-in restriction imposed on them. The resulting network is such that it minimizes the cost function $h(G, I)$, a monotone increasing function of $G$ and $I$, where $G$ is the total number of gates and $I$ is the total number of interconnections in the network. In other words, the earlier work is generalized so that the number of interconnections may be included in its cost criterion. The algorithm is then extended to the multiple output network design.

R-70-201. Christal, Wiley H. and Cole, Jack H. Synthesis of Asynchronous Sequential Electrical Logic Control Systems with Feedback Inputs. (35 pp.; Texas Instruments, Dallas, Texas) A procedure for synthesizing a logical sequential controller is presented. This procedure does not depend upon Karnaugh map simplification; therefore, the complexity of the controller is not a limitation. An algorithm is presented by means of an example in which controllers can be synthesized in one table — called the synthesis table. This synthesis procedure differs from other procedures by the use of memory functions. A passive distribution element, the Y-gate, is used as the memory function.

R-70-202. Perlowski, Andrew A. Minimization of the Boolean Function Using Digital Computer. (31 pp.; RCA, Palm Beach Gardens, Florida) An algorithm is developed for obtaining a minimum-gate network. The method of iterated consensus is used to implement the algorithm and a program for a digital computer is organized showing how the consensus and subsumption can be realized by use of machine language.

R-70-203. Baugh, C. R. Bounds on the Number of Pseudo-Threshold Functions. (22 pp.; Bell Telephone Laboratories, Holmdel, N.J.) Upper and lower bounds are derived for the number of pseudo-threshold functions of $n$ variables. (Pseudo-threshold logic is a generalization of threshold logic.) It is shown that the number of pseudo-threshold functions $P(n)$ of $n$ variables realized by zero-free structures is bounded by

$$\frac{2^{n-\frac{1}{2}}}{\sqrt{n}} + n < P(n) < \sqrt{\frac{2}{\pi n}} \left( \frac{e}{n} \right)^n \frac{n^2}{2 \sqrt{n}} + n^2$$
The number of pseudo-threshold functions $Q(n)$ of $n$ variables realized by nontrivial structures is bounded by

$$2^{n-1} - Q(n) \leq 2 \cdot 2^{n-1}$$

It is also proven that $Q(n) = 2^{n^2}$ is a lower bound on the number of positive functions.

R-70-204. Agarwal, Vijay K. A New Approach to the Fast Hadamard Transform Algorithm. (12 pp.; TRW Systems Group, Redondo Beach, Calif.)

Recently some researchers have discussed "fast" Hadamard transform algorithms that can be implemented to perform the one dimensional transform of a sequence of $N$-point Hadamard matrix with $N$ operations as opposed to the $N(N-1)$ operations required by more direct methods. Although they are all fast algorithms which perform the computations with $N$ log $N$ additions or subtractions, the chief criteria for selection between the various algorithms are the amount of "unnecessary" operations that must be performed and the amount of dynamic storage needed. An alternate and improved approach to performing a fast Hadamard transform is presented wherein advantage is taken of the repetitive structure of the operations. The entire algorithm reduces to simple matrix operations because the best factorization of the Hadamard factorable matrices can be obtained by the direct matrix product method. This approach, which is simpler and easier understood with a matrix theory background, gives results which are convenient for hardware implementation of a transform processor.

R-70-205. Smith, John R., Jr. and Roth, Charles H., Jr. Analysis and Synthesis of Asynchronous Sequential Networks Using Edge-Sensitive Flip-Flops. (36 pp.; University of Texas, Austin, Texas)

Standard switching table methods for analysis and synthesis of asynchronous sequential switching networks are difficult to apply when edge-sensitive flip-flops are used. Use of a differential mode (DM) state table, which specifies the next state as a function of the present state and input change, avoids such difficulties. Difference equations, which are used to specify changes in logic variables, provide a convenient means for defining terminal behavior of edge-sensitive flip-flops. The inhibited toggle flip-flop is introduced as a general-purpose edge-sensitive flip-flop. Sequential networks are analyzed by writing difference equations (from which the DM table can be constructed). Synthesis of asynchronous networks is accomplished by first constructing a DM table to describe the desired network behavior and then deriving input equations for inhibited-toggle flip-flops. Such realizations are free of hazards and critical races and usually require fewer gates and flip-flop delays than solutions by standard flow table methods.

R-70-206. Smith, John R., Jr. and Roth, Charles H., Jr. Differential Mode Sequential Machines. (35 pp.; University of Texas, Austin, Texas)

Some sequential networks containing edge-sensitive flip-flops cannot be directly analyzed by standard methods without introducing auxiliary state variables. The differential mode (DM) sequential machine serves as a model for such networks. The next state function for the DM machine expresses the next state in terms of input changes and state model of digital. Any fundamental mode asynchronous (FMA) machine can be converted to a DM machine which has the same behavior, but sometimes the DM machine requires fewer states. Any DM machine can be converted to an FMA machine which simulates the behavior of the DM machine; therefore, indirect realization of a DM machine is always possible.


This short note reports some experimental results pertaining to the statistics of terms (prime implicates, essential and inessential implicants, covering terms, etc.) characterizing switching functions and especially two-level minimization. In particular, it is shown that the statistical distribution of these terms resembles the Gaussian one and the diagrams of average values and variance versus number of inputs of minimum for functions in $6 \to 11$ variables are presented. The computations have been performed on a special-purpose computer, which was designed and constructed for purpose for this work.


The increasing complexity of digital systems over the past decade has been accompanied by a growing awareness of the need for efficient fault diagnosis, as proved by the ever increasing literature published on the subject. The paper is based on 86 referenced sources and its main function is to review the published methods of deriving diagnostic test sequences, indicating the advantages and disadvantages of each technique. In so doing, it traces the interaction between the diagnostic techniques that have evolved and their influence on the design philosophy of digital systems at all levels. It is apparent from the review that there exists a requirement for a unified theory of diagnosis compatible with, and complementary to current design techniques based on switching theory, and ways are suggested in which this might be achieved.


Parallel decimal arithmetic capability is becoming increasingly attractive with new applications of computers in a multiprogramming environment. The direct provision of decimal summing offers a significant improvement when addition over methods requiring decimal correction. These techniques are illustrated in the eight digit adder which appears in the System/360 Model 195.


This paper briefly explains the TRAC T-64 standard language and then covers several aspects of a new implementation for the DEC PDP-8 and PDP-9 class machines: 1. The TRAC T-64 language and its Primitive Function expressions. 2. Structure of the Active and Neutral Strings. 3. Structure of the Form Store. 4. Organization of the Processor. 5 Language extensions and Mode Switches.

R-70-211. King, Willis K. Design of an Associative Memory. (19 pp.; University of Houston, Houston, Texas)

An associative memory system using push-down or first-in-first-out (FIFO) lists as its basic building elements is described. With the development of Large Scale Integration technology (LSI) it is expected that devices with regular repetitive structure and high gate/interconnection ratio can be manufactured at extreme low cost. Pushdown and FIFO evidently belong to that category. The logical design of a push-down and a FIFO list memory are first described. Then with some additional control logic it is shown that they can be converted to an associative memory.


In this paper, automation of digital systems is studied. The aim of the research is to develop some tools for a digital system designer to perform his design with the aid of digital computers. A language which describes a digital system has been developed. By means of this language a digital system can be described on a level of detail specified by the designer. The language is based on a set of digital systems which separates the structure and control of the system to be designed. This simplifies the design process and enables the designer to specify his digital system precisely. A description of a digital system in this language consists of several subsystems (units) which are made of smaller modules. Each subsystem in the description has two main parts. The structure part and the control part. The structure part describes the hardware modules of which the system is made. These modules are of two kinds: operators and links. The operators are connected to each other via links. Operators are mainly combinational logic circuits. Links are either registers or terminals. The control part controls the actions (operations) of the structure part and decides on the next action (operation) to take. It consists of four different kinds of elements. One of these elements activates the operators in the structure part. The activated operator then maps the values at its input to obtain the appropriate output values corresponding to the values of control signals. Another type of element controls the sequence of operations and can transfer the control to various portions of the control part, depending on some values in the structure. The other two elements are used to describe parallel operations in a subsystem. The language based on this model is capable of describing hardware modules in the structure part and the control elements in the control part.

R-70-213. Chen, Wen-Fu and Glanz, Filson H. Realization of Non-1-Realizable Boolean Functions with Negative Threshold Networks. (35 pp.; University of New Hampshire, Durham, N.H.)

The purpose of this research is to generalize Dartozou’s THRESH-OR and THRESH-CASCADE methods for functional decomposition to include the negative input weight for connecting the output of one threshold gate to one input of another threshold gate, thus forming a threshold network for a non-1-realizable Boolean function. The addition of these two "NEGATIVE" THRESH-OLD methods can minimize the number of threshold gates required for realization and/or save realization times for some classes of functions in comparison with the results achievable by using "POSITIVE" THRESHOLD methods.

R-70-214. Harada, Kazuaki. Sequential Permutation Networks. (30 pp.; Washington University, St. Louis, Mo.)

Two sequential switching networks capable of permuting their $n$ input lines to their $n$ output lines in two different sequential cyclic manners covering all $n!$ permutations are presented. The networks are constructed in multiple cascade by $\frac{n}{n-1}$ switching elements of which permuting input pair to its output pair according to its internal state $(1,0)$. One of the networks is constructed and controlled referring to the principle which is based on a recursive application of product functions. The other is slightly modified and can produce permutations in lexicographic order. By factorial representation of integer $N$, $N = \sum_{h=1}^{n} h! S_{h} O_{h} = n! S_{n} \leq h$, the relationship among the $N^{+}$ permutation, factorial digit $S_{h}$ and the states of the switching elements in the network is established. The procedure is also given for setting
up the switching elements in the network according to any specified permutation matrix.


In studying automorphism groups of semiautomata, Bayer introduced a condition "state independence." This note gives a simpler equivalent condition called "symmetry." We also show that a symmetric semiautomaton is a direct sum of mutually isomorphic strongly connected semiautomata, and that one of Bayer's results can be strengthened somewhat.


Beretkamp's iterative algorithm (1) was introduced for decoding Bose-Chaudhuri-Hocquenghem codes. In this note we show that the algorithm may be used to design recursive filters with a bounded error response. Numerical results are also given.


A universal logic primitive (ULP) is a logic function by which every logic function of n variables is composed. The ULP's for n logic variables is derived and a procedure for determining all of them is presented.


This paper considers the use of N-valued logics in the design of base N adder circuits. Two types of N-valued logics are examined: Post N-valued logics and binary-coded N-valued logics. General formulas for the sum and carry functions of an adder are established in order to calculate the cost of base N adder stages using the Post Logics. Relative costs of the base N adders using both types of N-valued logics are discussed in terms of a cost function. It is shown that the binary-coded logics yield adders which, in general, lower relative cost than comparable adders based on the Post logics, and that base 2 adders have a lower relative cost than the base N adders.

R-70-219. Cantoni, A. Optimal Curve Fitting With Piecewise Linear Functions — III. (43 pp.; The University of Western Australia, Nedlands, Australia)

Two recent papers have described methods of finding a continuous piecewise-linear approximation to a specified function such that the weighted integral squared error over some finite interval is minimized. Extension of the methods to treat the case of a performance index defined over an infinite interval is considered and algorithms for determining the optimal solutions for certain classes of functions are described. The results obtained for some specific functions are included and discussed. Also considered are the various suboptimal solutions which can be obtained when constraints are imposed on the piecewise-linear approximation function.

R-70-220. Gouraud, Henri. Continuous Shading of Curved Surfaces. (34 pp.; University of Utah, Salt Lake City, Utah)

A procedure for computing shaded pictures of curved surfaces is presented. The surface is approximated by small polygons so that the discontinuities of shade are eliminated across the surface and a smooth appearance is obtained. In order to achieve speed efficiency, the technique developed by G. Watkins is used which makes possible a hardware implementation of this algorithm.

R-70-221. Srinivasan, C. V. Codes for Error Correction in High Speed Memory Systems. Part II: Correction of Temporary and Catastrophic Errors. (36 pp.; Rutgers University, New Brunswick, N.J.)

A few classes of codes, suitable for error correction in high speed memory systems, are presented. The codes have relatively simple parallel decoding nets. The codes may be used both for the correction of temporary and catastrophic errors.


The heavy maintainability requirements of the electronic computers implemented by integrated circuits result in the need of planning for adequate self-diagnostic tools since the design stage. Having identified as a significant parameter of such tools the capability for "Reliable fault isolation capability" up to the level of the minimum replaceable module, then the basic items of a self-diagnostic procedure are illustrated, such as the "stimuli," the "symptoms," and the "symptom-failure dictionary." Taking into consideration the peculiar problem of defining a system to provide digital equipment with automatic failure isolation capability, a critical review is made of the fault simulation techniques which support the self-diagnosis philosophy. Hence the specification of a novel method are established, as a combination of the positive features of the physical simulation and of the software simulation as well. Based on this method, the SAFE (Simulation Aided Fault Evaluation) System utilizes a computer in a two-fold function, i.e., in controlling the simulation process and in related data processing. The end result consists of the automatic generation of a symptom-failure dictionary associated to a simple procedure for applying the stimuli and observing the symptoms. Finally, the integrated hardware — software package of the SAFE System is illustrated along with its basic operating sequence; reference is made to application cases in the area of both Central Processing Units and Peripheral Subsystems.

R-70-223. Chiang, A. C. L. and Reed, I. S. Notes on the Arithmetic BN Modulo A Codes. (12 pp.; Macrodatal Company, Chatsworth, Calif.)

Properties of arithmetic norms of integers are applied to the study of arithmetic BN modulo A codes. Some new properties of such codes are established. Bounds on the size of such codes are derived and an efficient algorithm for finding the optimal single — and double — error — correcting BN modulo A codes is developed.

R-70-224. Suzuki, Y.; Pak, P.S.; and Fuji, K. Pseudo Gaussian Noise Generator. (47 pp.; Osaka University, Osaka, Japan)

This paper deals with a device which can generate a pseudo Gaussian white noise. This noise generator utilizes an artificial m-sequence signal as its noise source, so that it has very useful and convenient properties for various applications. For example, same output noise signal can be generated repeatedly and its time scale can be changed as user's will. A pseudo Gaussian white noise is obtained by adding a large number of replicas of the m-sequence signal whose phase differences are large and random one another. The configuration of the designed pseudo Gaussian noise generator is described. The statistical properties of the output signal and its filtered one are investigated experimentally, and are confirmed to be satisfactory.

R-70-225. Henderson, Keith W. Comments on "Realization of an Arbitrary Switching Function With a Two-Level Network of Threshold and Parity Elements." (5 pp.; Stanford Linear Accelerator Center, Stanford, Calif.)

Attention is called to previous research on realization of an arbitrary switching function by a network of threshold gates (or parity elements) and modulo — 2 gates (or parity elements), establishment of greatest lower bounds on the number of gates needed, systematic minimalization of the number of modulo — 2 gates required, and artifacts that lead to further network reduction in special cases. Although not widely published, a report describing the research in detail is readily available at a nominal price.

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