algorithms, directly in the language of the RGP. Using specialized circuitry, the RGP performs graphics clipping in parallel with the drawing operations. Thus this additional functionality is provided with no degradation in drawing performance.

National's DP8510 BPU (bitblt processing unit) is the slave data manipulator, operating at clock rates up to 20 MHz. It performs all of the masking, barrel shifting, data transfer, and Boolean logic necessary for bitblt operations. Any number of BPUs can be controlled by a single RGP, which allows the flexibility of using the same core architecture and software to design a family of products ranging from monochrome to 24 bits (or more) per pixel.

National's DP8512 VCG (video clock generator) is the timing and control generator for the graphics system. It provides system clocks at rates up to 20 MHz for the RGP and the BPUs. It also provides load clocks for controlling the parallel loading of the shift registers, as well as pixel clocks at rates up to 225 MHz for controlling shift-register serial output.

National's DP8515/16 VSR (video shift register) converts parallel data words from the frame buffer into a high-speed serial data stream for video input to the CRT at a maximum clock rate of 225 MHz. An on-board FIFO eases the system timing constraints encountered at these high clock rates.

The entire chip set has been designed to support all types of RAM components that might be used in the frame buffer, including static RAM, dynamic RAM, and video DRAM.

Summary

The National Semiconductor architecture is very well suited for plane-oriented architectures but can work equally well in pixel-oriented architectures. Additionally, it is the first chip set to provide a complete solution for mixed-mode applications. The flexibility and performance provided by the Advanced Graphics Chip Set ensure that it can be used for designing graphics hardware products well into the 1990's.

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