A Message from the New Editor-in-Chief and Introduction of New Associate Editors

José F. Martínez

My first submission experience to IEEE Computer Architecture Letters (CAL) was nothing like any other conference or journal submission before. Reviews were back in under a month, and yet they were thorough and insightful. The reviewers did not get lost in the evaluation details; instead, they zeroed in on the innovation, or as one reviewer put it, the “wow factor.” Yale Patt, the Editor-in-Chief (EIC) at the time, was exceedingly helpful and supportive.

A few years later, with CAL quickly gaining recognition in our research community, and with Kevin Skadron at the helm as new EIC, I was thrilled to join the Editorial Board as an Associate Editor. In 2011, I became Kevin’s sidekick as Associate EIC, and got to learn the ropes from a phenomenal leader. In 2012, when Kevin was about to become department chair at the University of Virginia, I agreed to step up as Acting EIC of CAL. Finally, in 2013, I started my tenure as CAL’s newest EIC.

I am humbled and excited about the prospect of leading CAL’s next phase. To say that I have big shoes to fill is a great understatement. Although it is a big responsibility, it was frankly easy to accept, given Kevin’s excellent mentoring, the outstanding composition of the Editorial Board, and the wonderfully competent and helpful staff at the IEEE Computer Society.

My goal during my tenure as CAL’s EIC will be to further increase its visibility in our research community, and to attract more submissions from computer architecture leaders. The “Best of CAL” session at HPCA, which has taken place for the last couple of years, is a good step in this direction. I am also committed to continue improving the coordination with authors and conference program chairs, and to consolidate CAL’s unique place in the publication pipeline as the prime venue for quick dissemination of high-quality novel ideas and early results.

To help me accomplish this, I am very fortunate to count on Lieven Eeckhout as CAL’s new Associate EIC. Lieven is of course a highly accomplished, award-winning architecture researcher, but he is also an extraordinarily prompt and thorough Associate Editor, and he has contributed significantly to initiatives such as “Best of CAL.”

I eagerly look forward to working with all of you to bring CAL to new levels of success and impact.

José F. Martínez
Editor-in-Chief

Lieven Eeckhout received the PhD degree from Ghent University, Belgium, in 2002. He is currently a professor at Ghent University. His main research interests include computer architecture and the hardware/software interface in general, and performance modeling and analysis, simulation methodology, and workload characterization in particular. He received two IEEE Micro Top Picks Awards for the year’s most significant research publications in computer architecture, received the best paper award at ISPASS 2013, and recently wrote a synthesis lecture on “Computer Architecture Performance Evaluation Methods” published by Morgan and Claypool. He has graduated 10 PhD students and currently supervises four postdoctoral researchers and eight PhD students. He has served on more than 40 technical program committees for top conferences, was the program chair for ISPASS 2009 and cochair for CGO 2013, and is an associate editor for the ACM Transactions on Architecture and Code Optimization, IEEE Micro, and the IEEE Computer Architecture Letters.

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Tor Aamodt received the BA Sc (in engineering science), MA Sc, and PhD degrees from the University of Toronto. He is an associate professor in the Department of Electrical and Computer Engineering at the University of British Columbia and a visiting associate professor in the Computer Science Department at Stanford University. His current research focuses on architecture and microarchitecture of manycore accelerators such as graphics processing units (GPUs), heterogeneous multicore processors, and analytical performance modeling of modern processor architectures. His research on hardware transactional memory on GPUs was selected as a “top pick” from computer architecture conferences by IEEE Micro magazine. He is an associate editor for the IEEE Computer Architecture Letters, program chair for ISPASS 2013, and has served on numerous program committees. As a graduate student, he spent about a year as an intern in Intel’s Microarchitecture Research Lab. He worked at NVIDIA on the GeForce 8 Series GPU, which was the first NVIDIA GPU to support CUDA.

Ricardo Bianchini received the PhD degree in computer science from the University of Rochester in 1995. From 1995 to 1999, he was an assistant professor at the Federal University of Rio de Janeiro, Brazil. He is now a professor with Rutgers University. His current research interests include the power, energy, and thermal management of data centers. In fact, he is a pioneer in data center energy management and energy-aware storage systems. He also introduced the Mercury tool for thermal emulation and many policies for handling thermal emergencies in data centers. He cochaired the program committees of two large conferences and has been a member of the program committee of more than 50 conferences and workshops. He is currently an associate editor for the IEEE Transactions on Parallel and Distributed Systems and a member of the editorial board for the Elsevier Journal of Systems and Software. He has also received many awards, including the US National Science Foundation CAREER award.

Chita R. Das received the MSc degree in electrical engineering from the Regional Engineering College, Rourkela, India, in 1981, and the PhD degree in computer science from the Center for Advanced Computer Studies, University of Louisiana, Lafayette, in 1986. Since 1986, he has been with the Pennsylvania State University, where he is currently a distinguished professor in the Department of Computer Science and Engineering. His main areas of interest are parallel and distributed computer architectures, cluster computing, mobile computing, Internet QoS, multimedia systems, performance evaluation, and fault-tolerant computing. He has published extensively in these areas. He has served on the editorial boards of the IEEE Transactions on Computers and IEEE Transactions on Parallel and Distributed Systems. He is a fellow of the IEEE and a member of the ACM.

José Flich received the PhD degree in 2001 in computer engineering. He is an associate professor at Universidad Politécnica de Valencia (UPV), where he leads the research activities related to on-chip networks. He has published more than 100 conference and journal papers, and has served on different conference program committees (ISCA, NOCS, DATE, ICPP, IPDPS, HiPC, CAC, CASS, IPCPADS, and ISCC), as program chair (INA-OCMC and CAC), and as track cochair (EUROPAR). He is an associate editor of the IEEE Transactions on Parallel and Distributed Systems. He has collaborated with different institutions (Ferrara, Catania, Jonkoping, and USC) and companies (AMD, Intel, and Sun). His current research activities focus on routing, coherency protocols, and congestion management within NoCs. He co-invented different routing strategies and reconfiguration and congestion control mechanisms, some of them with high recognition (RECN and LBDR for on-chip networks). He is a member of the Hipec-2 NoE. He is coeditor of the book Designing Network-on-Chip Architectures in the Nanoscale Era and the coordinator of the FP7 NaNoC project.

Idit Keidar received the BSc (summa cum laude), MSc (summa cum laude), and PhD degrees from the Hebrew University of Jerusalem. She is an associate professor in the Electrical Engineering Department of the Technion. She is a recipient of the National Allon Fellowship for new faculty members, the David Dudi Ben-Aharon Research Award, and the Muriel and David Jackow Award for Excellence in Teaching. She was a postdoctoral research associate at MIT’s Laboratory for Computer Science, where she held postdoctoral fellowships from Rothschild Yad-Hanadiv and the US National Science Foundation’s CISE. She has consulted for BBN Technologies (a Verizon company) in the area of fault-tolerance and intrusion tolerance, and for Microsoft Research in the area of fault-tolerant storage systems. She was a visiting professor at Cornell University. Her research is broadly in distributed and concurrent algorithms and systems, as well as fault-tolerant network-based computing. Her work combines theory and practice. Most recently, she has been interested in multicores (CMP), transactional memory and concurrent data structures, dynamic (reconfigurable) distributed storage, cloud storage, local computing and dynamic networks, and replication and coordination.
**EJ Kim** received the BS degree in computer science from the Korea Advanced Institute of Science and Technology in 1992, the MS degree in computer science and engineering from the Pohang University of Science and Technology in 1994, and the PhD degree in computer science and engineering from Pennsylvania State University in 2003. She has been an associate professor in the Department of Computer Science and Engineering at Texas A&M University since 2010. Prior to current appointment, she was a member of the technical staff in the Communication Network Research and Development Group at Korea Telecom from 1994-1997, a teaching assistant in the Department of Computer Science and Engineering at The Pennsylvania State University from 1998-1999, and a research assistant in the Department of Computer Science and Engineering at The Pennsylvania State University from 1999-2003. Her research interests are in computer architecture, power efficient systems, parallel/distributed systems, cluster computing, performance evaluation, and fault-tolerant computing. Her research has been supported by the US National Science Foundation (NSF), and she received the NSF Early CAREER Award in 2009.

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**Jun Yang** received the PhD degree in computer science from the University of Arizona in 2002. She is currently an associate professor of in the Electrical and Computer Engineering Department at the University of Pittsburgh. She was a recipient of the US National Science Foundation CAREER award in 2008. Her research interests include low power and temperature-aware microarchitecture designs, 3D integration, new memory technologies, and networks-on-chip.