

# Editorial: Letter from the Editor-in-Chief

Kevin Skadron

I'm pleased to welcome you to the latest issue of *IEEE Computer Architecture Letters (CAL)*. This issue includes papers with novel approaches to memory hierarchy, multithreading, and transactional memory.

I'd like to take this opportunity to share with you several important announcements. First, we recently learned that *CAL* is now indexed by the Thomson-Reuters' *Science Citation Index*, which recognizes us as one of the world's leading scientific and technical scholarly publications. This is only possible because of the high-quality submissions we receive and the careful evaluation and feedback performed by our reviewers and editorial board.

I am also pleased to announce that the 2012 IEEE International Symposium on High Performance Computer Architecture (HPCA) will feature a special session on the "Best Papers from *Computer Architecture Letters*" from 2011. All papers that were posted online or appeared in print in 2011 will be eligible, and the decision will be made by a committee of *CAL* and HPCA representatives. Authors of the selected papers will give a short presentation, a pamphlet with one-page extended abstracts for each selected paper will be distributed at the session, and there will be plenty of time for questions and discussion. Making this event part of the main program for HPCA will boost visibility for these selected papers and *CAL* as a whole. Many thanks to this year's HPCA organizers for making this possible.

Please welcome José Martínez as the new Associate Editor-in-Chief (AEIC) of *CAL*. He takes over from Sudhanva Gurumurthi, who moves to the editorial board. Many thanks to Sudhanva for his hard work as AEIC. He helped dramatically improve the timeliness of our review process and led the creation of a process by which we have started proactively encouraging the authors of the best early work from workshops to submit to *CAL*. These papers are then treated as regular submissions.

I would also like to welcome several new members of the editorial board: Jack Dongarra (U. Tennessee-Knoxville and Oak Ridge National Laboratory), Lieven Eeckhout (U. Ghent), Parthasarathy Ranganathan (HP Labs), Timothy Sherwood (U. California at Santa Barbara), and Sudhakar Yalamanchili (Georgia Institute of Technology). They are leaders in the field and contribute valuable expertise. At the same time, I would like to thank several members of the editorial board whose terms have expired due to term limits: Pradip Bose (IBM Research), Sandhya Dwarkadas (U. Rochester), Norm Jouppi (HP Labs), Walid Najjar (U. California at Riverside), Mateo Valero (U. Politècnica de Catalunya Barcelona), Uri Weiser (Technion), and Andrew Wolfe (independent consultant). I want to express my deepest thanks for their collective wisdom and hard work in helping make *CAL* a success.

Timeliness remains one of the hallmarks of *CAL*. So far in 2011, we have had 27 submissions, which is about the same pace as last year. The acceptance rate continues to be about 24 percent. Our turnaround time continues to stay close to our target of one month from submission to first decision. For our 2011 submissions so far, the mean turnaround time has been 27 days, with most papers meeting our one month target, and the maximum has been 38 days. However, we never want to sacrifice the quality of a decision for the sake of expediency, and prefer to take extra time when necessary to get an extra review or clarify some aspect of a review. Once a paper is accepted and the final camera-ready copy is submitted, it is posted immediately on the Computer Society Digital Library and forwarded to Xplore, where it appears under *CAL*'s "forthcoming" papers until it appears in print.

We look for papers that provide ideas or insights that are novel or likely to have lasting importance. We welcome papers presenting early work in new areas, and recognize that such work is also likely to provide only early evidence to support the paper's claims. Papers on more established topics are expected to be able to provide stronger evidence in support of their claims. We have recently revised our review form to better clarify these standards to our reviewers. It is also important to note that, since *CAL* actively encourages submissions of early work, we expect and hope that most work appearing in *CAL* will be extended and go on to full-length treatments in conferences or journals. There have been some questions about whether publishing in *CAL* could preclude such subsequent publication. In fact, many *CAL* papers have been extended and appeared in computer architecture's most prestigious conferences. However, to clarify any lingering questions, the IEEE Computer Society's Transactions Operating Committee, which governs *CAL* and its transactions, as well as ACM's and the IEEE Computer Society's special interest groups, SIGARCH and TCCA, which sponsor most of computer architecture's main conferences, have all stated policies that "a prior Letter paper should not bias reviewers' evaluation of a subsequent conference, transaction, or magazine submission," as long as sufficient new material is presented in the full-length version.

Sincerely,

Kevin Skadron  
Editor-in-Chief



**José Martínez** graduated in computer science and engineering in 1996 from the Universidad Politécnica de Valencia, and received the MS degree in 1999 and the PhD degree in 2002 in computer science from the University of Illinois at Urbana-Champaign. He is now an associate professor of electrical and computer engineering, as well as a graduate field member of computer science, at Cornell University, Ithaca, New York. His research work has earned several awards, among them two IEEE Micro Top Picks papers, an HPCA Best Paper Award, a US National Science Foundation CAREER Award, and two IBM Faculty Awards. On the teaching side, he was recognized with a 2005 Kenneth A. Goldman '71 Excellence in Teaching Award, as a 2007 Merrill Presidential Teacher, and as the 2011 Tau Beta Pi Professor of the Year in the College of Engineering. He is an associate editor for the *ACM Transactions on Computer Architecture and Code Optimization*. He is a senior member of the ACM and the IEEE.



**Jack Dongarra** holds an appointment as University Distinguished Professor of Computer Science in the Electrical Engineering and Computer Science Department at the University of Tennessee and holds the title of Distinguished Research Staff in the Computer Science and Mathematics Division at Oak Ridge National Laboratory (ORNL), Turing Fellow in the Computer Science and Mathematics Schools at the University of Manchester, and adjunct professor in the Computer Science Department at Rice University. He specializes in numerical algorithms in linear algebra, parallel computing, use of advanced-computer architectures, programming methodology, and tools for parallel computers. His research includes the development, testing, and documentation of high quality mathematical software. He has contributed to the design and implementation of the following open source software packages and systems: EISPACK, LINPACK, the BLAS, LAPACK, ScaLAPACK, Netlib, PVM, MPI, NetSolve, Top500, ATLAS, Open-MPI, and PAPI. He has published approximately 300 articles, papers, reports, and technical memoranda and is coauthor of several books. In 2004, he was awarded the IEEE Sid Fernbach Award for his contributions in the application of high performance computers using innovative approaches; in 2008, he was the recipient of the first IEEE Medal of Excellence in Scalable Computing; and in 2010, he was the first recipient of the SIAM Special Interest Group on Supercomputing's award for Career Achievement. He is a fellow of the AAAS, ACM, IEEE, and SIAM and a member of the National Academy of Engineering.



**Lieven Eeckhout** is an associate professor at Ghent University, Belgium. His main research interests include computer architecture and the hardware/software interface in general, performance modeling and analysis, simulation methodology, and workload characterization in particular. He was the program chair for ISPASS 2009 and the general chair for ISPASS 2010. He received two IEEE Micro Top Picks Awards and recently wrote a synthesis lecture on "Computer Architecture Performance Evaluation Methods," published by Morgan and Claypool. He has graduated seven PhD students, and currently supervises two postdoctoral researchers and seven PhD students. He participates in the ExaScience Lab, part of Intel Labs Europe, focusing on architectural simulation techniques for exascale systems, and he was recently awarded an ERC Starting Independent Researcher Grant.



**Partha Ranganathan** received the BTech degree from the Indian Institute of Technology, Madras, and the MS and PhD degrees from Rice University, Houston. He is now a distinguished technologist at Hewlett Packard Labs, where he currently leads a large initiative on future data-centric data centers. His research interests are in systems architecture and manageability, energy-efficiency, and systems modeling and evaluation. He has done extensive work in these areas, including key contributions around energy-aware user interfaces, heterogeneous multicore processors, power capping and power-aware server designs, federated enterprise power management, energy modeling and benchmarking, disaggregated blade server architectures, and, most recently, storage hierarchy and systems redesign for nonvolatile memory. He was also one of the primary developers of the publicly distributed Rice Simulator for ILP Multiprocessors (RSIM). Dr. Ranganathan's work has led to several commercial products and has been featured in various venues including the *Wall Street Journal*, *Business Week*, *San Francisco Chronicle*, *Times of India*, *Slashdot* (<http://slashdot.org>), *YouTube* (<http://www.youtube.com>), and *Tom's Hardware Guide* (<http://www.tomshardware.com>). Dr. Ranganathan has been named one of the world's top young innovators by MIT's *Technology Review*, and has been recognized with several other awards including Rice University's Outstanding Young Engineering Alumni award.



**Tim Sherwood** received the BS degree in computer science and engineering from the University of California, Davis in 1998 and the MS and PhD degrees in the same subject from the University of California, San Diego in 2003. He now specializes in hardware security and is an associate professor in the Computer Science and Electrical Engineering Department at the University of California, Santa Barbara (UCSB). Embedded systems found in aircraft controls and the financial industry often require a level of assurance far above the norm. Dr. Sherwood's group at UCSB is developing new programmable architectures and that allows for a true implementation-level analysis of both hardware and software noninterference that includes both timing and storage side-channels. In addition, over the past six years with UCSB, he has included developed software profiling/debugging peripherals, novel uses of 3D integrated circuits for security and introspection, whiteboard-based sketch computing, MEMS sensor closed-loop control architectures, and high-assurance hardware/software systems. On four separate occasions he has had his papers selected by industry and academia as an "IEEE Micro Top Pick," he is a recipient of a US National Science Foundation Career Award, and he has won numerous teaching awards including the Northrup Grumman Excellence in Teaching Award.



**Sudhakar Yalamanchili** received the PhD degree in electrical and computer engineering in 1984 from the University of Texas at Austin. Upon graduation, he joined Honeywell's Systems and Research Center in Minneapolis, Minnesota, working on embedded multiprocessor architectures. From 1984 to 1989, he served as an adjunct faculty member in the Department of Electrical Engineering at the University of Minnesota, and served on Honeywell's Program Technical Advisory Committee to the Microelectronics Technology Corporation (MSS). He joined the Electrical and Computer Engineering faculty at the Georgia Institute of Technology in 1989, where he is now a Joseph M. Pettit Professor of Computer Engineering. His current research interests lie in addressing the software challenges of heterogeneous architectures, scalable simulation infrastructures, and solutions to power and thermal issues in many core architectures and data centers. He currently serves as a codirector of the US National Science Foundation Industry University Research Center on Experimental Computer Systems (CERCS) and is a member of the Research Advisory Group to the HyperTransport Consortium. He is the author of *VHDL Starters Guide* (second edition, Prentice Hall, 2004) and *VHDL: From Simulation to Synthesis* (Prentice Hall, 2000), and a coauthor with J. Duato and L. Ni of *Interconnection Networks: An Engineering Approach* (Morgan Kaufman, 2003). Dr. Yalamanchili served as the chair of the Computer Engineering Technical Interest Group within the School of Electrical and Computer Engineering (2008-2010) and continues to contribute professionally with regular service on editorial boards and conference program committees. He has served as an associate editor for the *IEEE Transactions on Parallel and Distributed Systems* and the *IEEE Transactions on Computers*. His most recent service includes general cochair of the 2010 IEEE/ACM International Symposium on Microarchitecture (MICRO) and program committees for the 2011 International Symposium on Networks on Chip and 2010 IEEE Micro Top Picks from Computer Architecture Conferences.