CALL FOR PAPERS
Defect and Fault Tolerance in VLSI and Nanotechnology Systems
IEEE Transactions on Emerging Topics in Computing
Special Issue/Section

IEEE Transaction on Emerging Topics in Computing (TETC) seeks original manuscripts for a Special Issue/Section on Defect and Fault Tolerance in VLSI and Nanotechnology Systems scheduled to appear in the last issue of 2016.

The continuous scaling of CMOS devices as well as the increased interest in the use of emerging technologies make more and more important the topics related to defect and fault tolerance in VLSI and nanotechnology systems. All aspects of design, manufacturing, test, reliability, and availability that are affected by defects during manufacturing and by faults during system operation, are of interest. The IEEE Transaction on Emerging Topics in Computing (TETC) seeks original manuscripts for a Special Section on Defect and Fault Tolerance in VLSI Systems scheduled to appear in the December issue of 2016. The topics of interest for this special issue include, but are not limited to:

1. **Yield Analysis and Modeling**: Defect/fault analysis and models; statistical yield modeling; critical area and metrics.
2. **Testing Techniques**: Built-in self-test; delay fault modeling and diagnosis; testing for analog and mixed circuits; signal and clock integrity.
4. **Error Detection, Correction, and Recovery**: Self-testing and self-checking solutions; error-control coding; fault masking and avoidance; recovery schemes, space/time redundancy; hardware/software techniques.
5. **Dependability Analysis and Validation**: Fault injection techniques and environments; dependability characterization.
6. **Repair, Restructuring and Reconfiguration**: Repairable logic; reconfigurable circuit design; DFT for on-line operation; self-healing.
7. **Defect and Fault Tolerance**: Reliable circuit/system synthesis; radiation hardened and/or tolerant processes & design; design space exploration for dependable systems, transient/soft faults and errors; Performance, power, reliability tradeoffs.
8. **Totally Fail-Safe Design for Critical Applications**: Methodologies and case study applications to automotive, railway, avionics, industrial control, biomedicine, space and smart power networks.
9. **Emerging Technologies**: Techniques for CNTs, QCA, DNA, RTDs, SETs, molecular devices and self-assembly.
10. **Hardware Security**: Fault attacks, fault tolerance-based counter-measures, Scan-based attacks and counter-measures, hardware trojans, security versus reliability tradeoffs, interaction between VLSI test, trust, and reliability.

Other topics related to reliable and resilient computing.

Submitted articles must describe original research which is not published nor currently under review by other journals or conferences. Extended conference papers should contain at least 40% new material and will pass through the normal review process. As an author, you are responsible for understanding and adhering to our submission guidelines. You can access them at the IEEE Computer Society web site, www.computer.org. Please thoroughly read these before submitting your manuscript. TETC is the newest Transactions of the IEEE Computer Society with hybrid open access publishing model.

Please submit your paper to Manuscript Central at https://mc.manuscriptcentral.com/tetc-cs

Please note the following important dates.
- **Submission Deadline**: December 1, 2015
- **Reviews Completed**: March 1, 2016
- **Major Revisions Due (if Needed)**: April 1, 2016
- **Reviews of Revisions Completed (if Needed)**: May 1, 2016
- **Minor Revisions Due (if Needed)**: June 1, 2016
- **Notification of Final Acceptance**: August 1, 2016
- **Publication Materials for Final Manuscripts Due**: September 1, 2016
- **Publication date**: Last Issue of 2016 (Dec Issue)

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