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The VLSI Circuits and Systems Letter is affiliated with the Technical Committee on VLSI (TCVLSI) under the IEEE Computer Society. It aims to report recent advances in VLSI technology, education and opportunities and, consequently, grow the research and education activities in the area. The letter covers the design methodologies for advanced VLSI circuit and systems, including digital circuits and systems, analog and radio-frequency circuits, as well as mixed-signal circuits and systems. It was published twice a year. Starting from this year, we will publish three issues per year in order to meet the high demand from our community.

TCVLSI focuses on integrating the design, computer-aided design, fabrication, application, and business aspects of VLSI while encompassing both hardware and software. It sponsors a number of premium conferences and workshops, including, but not limited to, ASAP, ASYNC, ISVLSI, IWLS, SLIP, and ARITH. Emerging research topics and state-of-the-art advances on VLSI circuits and systems are reported at these events on a regular basis. Best paper awards are selected at these conferences to promote the high-quality research work each year. In addition to these research activities, TCVLSI also supports a variety of educational activities related to TCVLSI. Several student travel grants are sponsored by TCVLSI in the following meetings: ASAP 2017, ISVLSI 2017, IWLS 2017, and SLIP 2017. Funds are provided to compensate student travels to these meetings as well as attract more student participation. The organizing committees of these meetings undertake the task of selecting right candidates for these awards.

This issue of the VLSI Circuits and Systems Letter showcases the state-of-the-art developments covering several emerging areas: customizable controller, nanoscale memory and cyber-physical system. Professional articles are solicited from technical experts to provide an in-depth review of these areas. The articles can be found in the sections of “Features” and “Opinions”. In the section of “Updates”, upcoming conferences/workshops (including their call for papers), funding opportunities, fellowship programs and job openings are summarized. Finally, a dedicated section of “Outreach and Community” discusses the approaches for outreach with successful stories.

We would like to express our great appreciation to all Associate Editors (Mike Borowczak, Prasun Ghosal, Shiyan Hu, Michael Hübner, Helen Li, Jawar Singh, Anirban Sengupta, Saket Srivastava, Yiyu Shi, Jun Tao and Qi Zhu) for their dedicated effort and strong support in organizing this letter. The complete editorial board information is available at: http://www.tcvlsi.org/vlsi-circuits-and-systems-letter/editorial-board/. For a quick reference the editorial board biography has been presented in this issue. We are thankful to our web chair Mike Borowczak, for his professional service to make the letter publically available on the Internet. We wish to thank Saket Srivastava, Adam Taylor, Stuart Smith, Pooran Singh, Santosh Kumar Vishvakarma, Qi Zhu and Wenchao Li who have contributed their professional articles to this issue. We hope that you will have an enjoyable moment when reading the letter! The call for contributions for the next issue is available at the end of this issue and we encourage you to submit articles, news, etc. to an associate editor covering that scope.

- Editors (Saraju Mohanty and Xin Li)
Features

High Level Design of a customizable CubeSat controller for micro/nano satellites
Saket Srivastava¹, Adam Taylor² and Stuart Smith²
¹School of Engineering, University of Lincoln, Brayford Pool, Lincoln, UK
²Lincoln DSP Limited, Maidstone, UK

Abstract – CubeSat and Small satellites are one of the fastest growing areas of space development in recent years. In this paper, we present a development methodology for a high performance, high reliability, lower power, highly customisable CubeSat controller module. Our proposed controller will significantly reduce the time to market and be suitable for use in other classes of nano/micro satellites. To the best of our knowledge no such capability exists, although some companies in Europe and USA offer lower performance modules, which constrain the user with a partial solution and more difficult programming and development environment.

Introduction

Small satellites, known as micro, nano or CubeSats, are defined as extremely small (10×10m×10n cm volume and 1-10kg mass, where n and m is between 1 and 3) spacecraft [1][2][3]. These satellites are launched on-board a space vehicle in a simple but effective dispenser, known as the “Poly-Picosatellite Orbital Deployer” (PPOD) [4][5]. This cost-effective launch technology has led to a rapid growth in recent years towards the commercialisation of these satellites to be used for a variety of applications such as telecom services, and low earth observation [6]. This commercialisation also puts pressures on the existing supply chain as operators demand higher performance, increased reliability and lower power consumption for their satellites. The commercialisation revenue stream dependency brings with it significant time pressures to achieve time to market (in this case launch).

The time duration it takes to design a micro/nano satellite is still a big bottleneck in the rapid advancement of this technology. A CubeSat development road map is shown in Figure 1. Each of the building blocks depicted in the road map are generally developed from scratch which prolongs the design, development and testing phase manifold. Even though many of the micro/nano satellites are designed for similar applications, there are still not many off the shelf customisable components available for CubeSat design and development. Our proposed controller module, which will form an integral part of a complete satellite system, is a step this direction.

![Figure 1 Development Road Map for a CubeSat](image_url)

CubeSats have traditionally used low performance microprocessors and paid little attention to design reliability except for some basic heritage evidence on device survivability. The move to commercialized CubeSats requires not only...
the consideration of reliability, but also introduces the need for performance increases without considerable effect on the power dissipation. We propose a design solution for a high performance, high reliability, lower power, highly customisable CubeSat controller, which will significantly reduce the time to market and be suitable for use in other classes of nano/micro satellites. Our proposed design is developed on a Xilinx Zynq based System on Chip (SoC) board to enable the function of the board to be defined by the user using a high-level software language without the need to be an expert in the lower level languages usually required to realize a full design. Some commercial solutions do offer lower performance modules on older Xilinx platforms. However, these solutions lack the high performance offered by the Zynq platform and constrain the user with a partial solution that is not easy to program and configure during the design and development phase [7][8].

**Design Approach**

The objective of this project is to develop a controller module with a high performance-processing core capable of operating as either a satellite platform controller or a payload instrument controller.

- The initial step in the design of CubeSat controller is to develop a system level specification for the all the elements of the CubeSat module given in Figure 1.
- Next step would be the development of detailed specification for the controller module, imaging module and the power supply.
- Based on the detailed specifications, an appropriate development platform can be chosen.
- As an example, a CubeSat controller module that was developed for an imaging satellite, utilises a Xilinx Zynq based System on Chip (SoC) platform as shown in Figure 2.

**Implementation Model**

Traditional CubeSat solutions have utilized low performance microprocessors that had low design reliability except for some basic heritage evidence on device survivability [9]. The move towards commercialized CubeSat’s requires, not only the consideration of reliability, but also the need for performance enhancement without considerably affecting the power requirements [10].
The user can use both the FPGA and processors combined within the SoC, however, all the design is developed in software, within a virtual system environment with functions accelerated as defined by the Xilinx Software Defined system level synthesis tool (SDSoC) which enables functions to be off loaded seamlessly to the programmable logic at the click of a software switch in the development tool [12]. SDSoC allows the system providers to provide the reliable modules required in the programmable logic to achieve the reliability and specific interfacing requirements for the platform. This provides the user with the ability to receive the benefits of the acceleration from the programmable logic without the need to develop in Verilog/VHDL as highlighted in Figure 4.

Figure 4: Illustration of separation of user development and layer to be developed on this project
To enable the use of SDSoC one of the outputs from this development will be the SDSoC platform which contains the reliable interfaces and board control and monitoring logic to enable the user to accelerate their function without the need to consider this aspect of the design. This application will use the built-in capabilities of the Zynq to provide a secure application enabling customer’s applications to be secure from reverse engineering or malicious interference. This will be enabled using AES 256 encryption of the boot image, RSA and HMAC verification of the images and ARM trust one technology which creates parallel software worlds for the underlying hardware. This technique prevents any interaction between the secure and non-secure elements of the design.

**Conclusion**

We have proposed a high performance, high reliability, lower power, highly customisable CubeSat controller for satellite applications. The proposed controller module is built using the Xilinx Zynq SoC platform and is configurable at the high level software language layer, removing the need for a detailed knowledge of FPGAs. Our proposed solution will significantly reduce the time to market and also be suitable for use in other classes of nano and micro satellites. This will further result in reducing the cost and expanding the CubeSat design and launch market manifold.

**Reference**

Differential dynamic feedback controlled 10T SRAM for ultra-low power applications

Pooran Singh and Santosh Kumar Vishvakarma
Nanoscale Devices, VLSI Circuit and System Design Lab, Discipline of Electrical Engineering, Indian Institute of Technology (IIT), Indore, MP, India

Abstract: The conventional 6T and read decoupled 8T SRAM cells are susceptible to craft enhanced stability and low leakage power while operating in ultra low voltages (ULVs). As a result, this paper demonstrates a differential dynamic feedback controlled 10T (DPFC10T) static random access memory (SRAM) cell to improve leakage power with better cell stability in subthreshold regions. The proposed 4Kb SRAM array show superior results in terms of write static noise margin (WSNM) by 1.66×, 1.44×, 1.83× and 1.49×; read static noise margin (RSNM) by 3.8×, 3.8×, 1.37× and 1.3×; write trip point (WTP) by 2×, 1.87×, 2× and 1.78× as compared to conventional 6T, differential data aware power supplied (D2AP)8T, low power (LP)8T and Schmitt trigger (ST)10T SRAMs, respectively at 300mV supply.

Keywords: SRAM, Dynamic feedback controlling, Leakage power, Read static noise margin (RSNM), Write trip point (WTP).

1. Introduction

Leakage power and cell stability are the key concern in sub-nanometre subthreshold SRAM architectures. SRAM cells are in hold state for most of the time, which causes leakage power as a major concern to look after. Nevertheless, portable electronic devices have extremely low power requirements to increase the battery lifetime. The cell stability is also a foremost concern at subthreshold power supply. The noise generated from threshold variation, process variation, half selected issue and multiple bit errors reduces stability of SRAM cell. Consequently, various techniques have been employed to overcome those limitations, such as scaling the supply voltage using process variation tolerant schmitt trigger based ST10T SRAM [1], a read static noise margin free 7T SRAM [2], differential data aware power supplied D2AP8T SRAM [3] and low leakage variation tolerant LP8T SRAM cell for ultralow power applications [4]. Besides the advantages provided by these cells, there are some limitations like low write-ability, consequences of process voltage temperature (PVT) variations, low write trip point (WTP) and higher power delay product (PDP) in subthreshold regions.

The SRAM is known as a power hungry device due to its high bit-line capacitances. In addition, the SRAM has tendency to fail at subthreshold voltages and shows vulnerability at various process voltage temperature (PVT) conditions. Therefore, to achieve less standby power various subthreshold SRAM cells have been proposed in literature [5-9]. The cell stability is also considered as one of the major concern in SRAM cell architectures. The read static noise margin (RSNM) can be improved using read decoupled logic [10]. Although, it is observed that read static noise margin (RSNM) is vulnerable at subthreshold regions while reading through full swing sense amplifier (SA) [11]-[13]. To compensate all these factors along with low leakage power and better cell stability, a differential DPFC10T SRAM cell is proposed in this paper.

2. Proposed DPFC10T SRAM

A DPFC10T SRAM cell in UMC 65nm technology is proposed in this paper. The cell works on feedback controlling of SRAM latch using two control inputs CS1 and CS2 as shown in Fig. 1(a) along with layout of proposed cell in Fig. 1(b). The write bitlines $WBL$ and $WBLB$ are for writing the information into the SRAM cell. Similarly, the read bitlines $RBL$ and $RBLB$ are for reading the information stored in the cell. The write and read operation is controlled by write and read access transistors M1-M2 and M9-M10, respectively. The positive feedback controlling is advances through two NMOS transistors M5 and M6. These two transistors are activated by control signals CS1 and CS2, which helps to improve the read-write speed, static noise margins and leakage power of the cell. The operations at different states are explained in Table 1.

A. Write operation

For write operation, write word line ($WWL$) must kept HIGH and the read word line ($RWL$) LOW. To write logic 1, the control signal CS1 is kept LOW and CS2 HIGH. Thus by keeping CS1 LOW, the transistor M5 gets OFF, which would
disconnect the discharging path through \( Q \). As a result, the storage node \( Q \) would charge fast through \( WBL \). Similarly, at storage node \( QB \), the M6 gets turned ON by asserting \( CS2 \) HIGH, which makes the discharging path across \( QB \) to GND. Therefore, information stored at \( QB \) would discharge quickly, which makes write 0 through \( WBLB \) fast. This also helps to improve the WSNM, since M5 turned OFF by asserting \( CS1 \) LOW in write 1 operation and if there would be any positive noise added at node \( QB \), which consequently turns ON M7. But due to slicing of discharging path of node \( Q \) through M5, it remains at logic 1.

Figure 1. (a) Schematic of proposed positive feedback controlled 10T (DPFC10T) SRAM cell. (b) Layout of proposed DPFC10T SRAM cell.

Table 1. Truth Table of Various Operations in Proposed DPFC10T SRAM.

<table>
<thead>
<tr>
<th>Operation</th>
<th>WW</th>
<th>RWL</th>
<th>WBL</th>
<th>WBLB</th>
<th>RBL</th>
<th>RBLB</th>
<th>CS1</th>
<th>CS2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Write 1</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Write 0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Read 1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Discharge</td>
<td>Discharge</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Read 0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Discharge</td>
<td>Discharge</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>Hold 1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Precharge</td>
<td>Precharge</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>Hold 0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Precharge</td>
<td>Precharge</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

B. Read operation

Before reading information from \( RBL \) and \( RBLB \), both are Precharge to VDD. Read operation is performed by keeping \( RWL \) to HIGH and \( WWL \) to LOW. For read 1 operation the control signals \( CS1 \) and \( CS2 \) are kept at logic 0 and logic 1 respectively. If logic 1 is stored at storage node \( Q \) and \( RWL \) is HIGH, which turn ON M9 and M10. Logic 1 at \( Q \) turns M8 ON and a discharging path from RBLB-M10-M8-GND is formed. The voltage difference, \( \Delta V_{RBL} = \{VDD - VDD - I_{\text{read}} \times R_{M8,M10}\} \) appears between \( RBL \) and \( RBLB \) to be sensed by sense amplifier (SA) [14]. Where \( I_{\text{read}} \) is the cell current and \( R_{M8,M10} \) is the resistance through M8 and M10. The control signal must be kept in pertinent state for all operations. To ensure this, only one information either logic 1 or logic 0 must be written in one column of an array. Therefore, in hold and read operation the control signal \( CS1 \) and \( CS2 \) are kept in similar state as assigned as in writing mode earlier.

C. Hold operation and leakage power

Hold operation is the state in which there would be no read- write operation take place in SRAM cell. Inevitably, the memory cell would remain in static or hold state most of the time. Thus, there would be very high possibility of increase in leakage power in SRAM cell. In proposed DPFC10T SRAM cell the control signal \( CS1 \) and \( CS2 \) help to reduce the leakage current by disconnecting the path of one of the inverters of the latch. As a result, in hold 1 state, at storage node \( Q \) the leakage path from VDD to GND is disconnected by turning M5 OFF through control signal \( CS1 \). Similarly, in hold 0 the leakage path is sliced by turning M6 OFF through \( CS2 \). This would reduce the leakage power addressed in subthreshold SRAM cells. The leakage power shown by the Gaussian curve at different temperature values in Fig. 2(a) and compared with the curve of C6T SRAM in Fig. 2(b). It demonstrates that the proposed cell has narrower spread of leakage power at 300mV VDD. Fig. 3 shows the sigma and mean value of leakage power of proposed 10T at different temperature. It shows that the proposed cell reaches to maximum of 1nW leakage power at 100°C of temperature.
D. Static Noise Margin (SNM)

Irrefutably, in read, write and hold 0 operations nodes Q and QB are at logic 0 and logic 1 state, respectively. Considerably, Q will turn OFF M8 and QB will turn ON M7. In conventional 6T SRAM or in other non-feedback controlled SRAM cells a noise will be added at Q or QB, which would flip the state of opposite storage node causing shrink to RSNM, HSNM and WSNM values. Moreover, in proposed PFC10T SRAM cell for read, write and hold 0 operations with CS2=0 will turn M6 OFF, which further disconnects the path from QB to GND through QB-M6-M8-GND. This helps to improve the SNM as CS2 control signal separates the discharging path of node QB=1 from GND. Consequently, QB will remain at logic 1 value instead of a positive noise added at Q.

E. Half selected issue

Half-selected column and row cells require a careful investigation under write operation [15]. Fig. 4(a) shows column half select write issue at 300mV VDD under write operation. It shows there would be no effect of half select write in the storage nodes of proposed cell. However, due row half select write issue at 300mV VDD as shown in Fig. 4(b), a positive voltage bump is generated at unselected cell for write operation when WWL switches from LOW to HIGH.

![Figure 2](image2.png)

Figure 2. (a) Leakage power of proposed cell through Gaussian curve at various temperatures (b) Leakage power of 6T through Gaussian curve at various temperatures.

![Figure 3](image3.png)

Figure 3. Mean (µ) and sigma (σ) values of leakage power of proposed cell at various temperatures.
3. Results and discussion for 4-Kb SRAM Macro

A DPFC10T SRAM cell based 4Kb array is designed in UMC 65nm technology and the post-layout simulation results are taken at different process voltage temperature (PVT) variations at 1000 Monte Carlo iterations. In write, hold and read 1 operation CS1 is kept at LOW and CS2 at HIGH and vice versa. Fig. 5(a) and Fig. 5(b) show the comparison of cell current and leakage current at different supply voltages respectively. The cell current or read current is observed through read bitlines (RBL or RBLB) at the time of read operation and the results shows analogous results as compared to existing cells. However, the leakage current is observed while the cell is at hold state. The leakage is reduced by cutting the VDD to GND path of one of the inverter of SRAM latch. The result shows a drastic reduction in leakage current. Fig. 5(c) shows that the $I_{on}/I_{off}$ value, which is the ratio between the cell current and the leakage current. The result shows huge improvement in ON-OFF current ratio as compared to other SRAM and similar value as LP8T SRAM [4]. Further, the read-write SNM is improved by the feedback cutting of one of the inverters of latch. Fig. 6(a) and Fig. 6(b) show the comparison of RSWM values at 300mV VDD and RSWM at different supply voltages, respectively as compared to existing SRAM. The results show an enormous amount of development in RSWM as compared to other cells. Fig. 7(a) demonstrates a comparison of WSNM at different subthreshold power supply voltages as compared to other cells. The WSNM at 300mV comes out to be 216mV which shows an improvement in a greater extant. Fig. 7(b) shows that the comparison of WTP/VDD percentage value. The WTP defines the write-ability of SRAM. The WTP/VDD % values of proposed cell has comes out to be more than 50%, which shows it has superior resilience against the noise added to the bitlines while writing into cell. Fig. 8(a) illustrates a comparison plot of leakage power consumption at different supply voltages. The proposed cell exhibits least leakage power at different voltage ranges. Further, Fig. 8(b) shows the leakage power at different temperature values. It depicts that the proposed cell has very less impact on increasing leakage power w.r.t. temperature. Fig. 8(c) shows the effect of process variations in leakage power, which doesn’t show much consequence on leakage power. The worst case leakage power has observed at fast slow (FS). Table 2 shows the summary of mean ($\mu$) values observed through 10,000 post-layout simulation iterations of proposed DPFC10T SRAM 4-Kb array at 300mV power supply. The parameters are observed at 27°C room temperature. It shows improvement in RSWM, WSNM, WTP, leakage power, $I_{on}/I_{off}$ value and PDP. The proposed cell WSNM is improved by 1.66×, 1.44×, 1.83× and 1.49×; RSWM by 3.8×, 3.8×, 1.37× and 1.3×; WTP by 2×, 1.87×, 2× and 1.78× as compared to conventional 6T, D2AP8T, LP8T and ST10T SRAMs, respectively. The power delay PDP is reduced to 0.28×, 0.7×, 0.55× and 0.63×; the leakage power also comes to 0.007×, 0.7×, 1.3× and 0.0125× as compared conventional 6T, D2AP8T, LP8T and ST10T SRAMs respectively. The proposed cell also shows better $I_{on}/I_{off}$ ratio by 74.56×, 36×, 1.55× and 50× as compared to 6T, 7T, D2AP8T and ST10T SRAMs respectively. From the table it can be observed that the goal of the proposed cell to reduce leakage power with better stability has achieved in accordance with maintaining process voltage temperature (PVT) parameters.
Figure 5. (a) Cell current or read current. (b) Leakage current at different supply voltages. (c) Cell current to leakage current ratio ($I_{on}/I_{off}$) at different supply voltages.

Figure 6. (a) Comparison of read static noise margin (RSNM) at 300mV VDD. (b) Comparison of read static noise margin at different supply voltages.

Figure 7. (a) Comparison of write static noise margin at 300mv VDD. (b) Comparison of write trip point (WTP)/ VDD % at various supply voltages.
Summary of Results of 4-Kb SRAM Mean (µ) Values of Post-Layout Simulation Results Taken at 1000 Monte Carlo Iterations at 300mV VDD

<table>
<thead>
<tr>
<th>SRAM</th>
<th>Parameter</th>
<th>WSNM (mV)</th>
<th>RSNM (mV)</th>
<th>WTP (mV)</th>
<th>Leakage Power</th>
<th>Ion/loff</th>
<th>Write1 delay (ns)</th>
<th>Write1 PDP (fJ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>C6T</td>
<td></td>
<td>130</td>
<td>36</td>
<td>81.3</td>
<td>12.8nW</td>
<td>22.13</td>
<td>8.133</td>
<td>0.246</td>
</tr>
<tr>
<td>7T</td>
<td></td>
<td>172</td>
<td>12</td>
<td>153</td>
<td>11.8nW</td>
<td>45.87</td>
<td>8</td>
<td>0.095</td>
</tr>
<tr>
<td>D2AP8T</td>
<td></td>
<td>150</td>
<td>35</td>
<td>89</td>
<td>14.2pW</td>
<td>1060</td>
<td>8.5</td>
<td>0.1</td>
</tr>
<tr>
<td>LP8T</td>
<td></td>
<td>118</td>
<td>100</td>
<td>82</td>
<td>7.6spW</td>
<td>3130</td>
<td>11.77</td>
<td>0.126</td>
</tr>
<tr>
<td>ST10T</td>
<td></td>
<td>145</td>
<td>105</td>
<td>93.2</td>
<td>0.8nW</td>
<td>34</td>
<td>8.89</td>
<td>0.11</td>
</tr>
<tr>
<td>DPFC10T</td>
<td></td>
<td>216</td>
<td>137</td>
<td>166.5</td>
<td>10pW</td>
<td>1650</td>
<td>9</td>
<td>0.07</td>
</tr>
</tbody>
</table>

Figure 8. (a) Comparison of leakage power at various supply voltages. (b) Comparison of leakage power at different temperature values. (c) Leakage power at different process corners.

4. Conclusion

A differential positive feedback controlled 10T SRAM is proposed in UMC 65nm technology. It shows better results in terms of RSNM, WSNM, leakage power, WTP and PDP. Proposed cell works on the principle of feedback cutting mechanism, in which one of the inverters of the SRAM latch VDD-GND path is disconnected using control signal C1 and C2 to improve stability and leakage power. Relatively it takes 45% more die area as compared to C6T SRAM but the low leakage and better cell stability makes DPFC10T a strong contender for future ULV/ULP internet of things (IoT) SRAM architectures.

References


Opinions

Extensibility Needs and Challenges for Cyber-Physical Systems

Qi Zhu, Department of Electrical and Computer Engineering, University of California, Riverside
Wenchao Li, Department of Electrical and Computer Engineering, Boston University

Abstract – Cyber-physical systems (CPSs) such as autonomous and semi-autonomous cars, tele-surgery robots, smart buildings, and factory automation systems, are poised to bring immense economic and societal benefits. However, the design and operation of CPSs still face tremendous challenges. One problem that stands out is the ineffectiveness in coping with software and hardware evolutions over the lifetime of a design or across multiple versions in the same product family. This problem has often caused significant delays of much needed updates. There is an urgent need for new design methodologies and tools to address the extensibility challenges in CPS.

Extensibility needs and challenges – Many CPS designs require continuous software and hardware updates over their lifetime for adding new functionality and features, modifying existing functionality and fixing bugs, or providing multiple versions as a product family to address different needs on performance, cost and operating environment. Such updates face significant challenges as the designers need to ensure both implementation feasibility and functional correctness. Without proper design automation tools for producing extensible initial designs and guiding updates, the redesign and re-verification cost often becomes prohibitive and greatly undermines system availability and reliability.

Using the automotive domain as an example, 90% of innovations in 2012 featured software and electronics, and it is predicted that the trend will continue in the future. Various features are added to the same platform through software and hardware to produce different models in a product line [1]. Furthermore, over the lifetime of the same model or even the same car, there are often incremental evolutionary changes throughout, such as adding new application software, reallocating some software among ECUs (Electronic Control Units), changing the connection of a sensor from one ECU to another, or adding a new ECU. These updates are needed to fix bugs (about 50% of car warranty costs are related to electronics and software; and sometimes multiple updates are required to fix one bug), and provide new functionality (some new features can even be added through remote software updates as with Tesla).

Attributes being considered in those updates include time, cost, system safety, reliability, availability, robustness, etc. The need for extensible designs is critical. As pointed out in [1] by an automotive architect, such process only works well “when new functionality can be absorbed by the architecture without the need of large changes”. However, achieving extensibility has become increasingly challenging, with exponentially growing number of features [2], stringent and diverse design requirements, limited resources, and more complex software and hardware architecture. In particular, the traditional federated architecture, where each function is deployed to one ECU and provided as a black-box by a Tier-1 supplier, is shifting to the integrated architecture, in which one function can be distributed over multiple ECUs and multiple functions can be supported by one ECU. This leads to significantly more resource sharing and contention among software functions, and greatly increases the complexity of finding extensible designs and validating updates.

For instance, as cyber-security emerges as a pressing issue for automotive systems, adding security mechanisms to existing designs is being investigated in academia and industry. In our previous work, we proposed formulations and algorithms for adding message authentication to the currently prevalent CAN (Controller Area Networks) architecture [3] and to the next generation TDMA (time division multiple access) based architecture [4]. For the resource-limited CAN architecture, we found that it is often difficult to add security updates, especially when the initial designs did not consider future extensions. Even for TDMA-based architecture with more bandwidth and faster speed, adding security updates has a complex impact on system schedulability and may lead to timing violations. It is therefore critical to develop methodologies for quantitatively analyzing such updates and guiding the design of extensible systems. This is particularly important for future automotive systems, as they become more connected with each other and with surrounding infrastructure, which will lead to more security vulnerabilities and frequent security updates [5].

Other CPSs, such as the SCADA (Supervisory Control and Data Acquisition) systems for industrial control in power plants, chemical plants and oil refineries, also face cyber-security threats and are in need of security updates in software and hardware. Note that just as automotive systems, malicious adversaries are adaptive and hence any fixed and static
solutions in dealing with such adversaries will deteriorate in efficacy over time. Therefore, such systems must be extensible to accommodate new updates to detect threat conditions and take appropriate remedial actions in real-time.

In some cases, driven by technological and economic incentives, a CPS design may be updated with new hardware components such as new CPUs or sensors. These updates may lead to changes of system timing behavior and affect various functional properties (note that even when everything runs faster with a more advanced CPU, possible changes in the event sequence and interaction with the physical environment might still cause problems). Analyzing these timing behavior changes is challenging, particularly while the systems move towards integrated architecture and multicore processors in the automotive and avionics domains. Currently, to avoid having to re-certify the software under hardware changes, aircraft manufactures often have to stockpile the electronic parts needed for the entire production line of an aircraft model [6], which greatly hinders the technology advancement of the system.

Related work – There has been a number of works addressing extensibility at the software task level [7]– [11]. In [9][11], extensibility is studied at the task level, but no explicit system synthesis is conducted. In [10], sensitivity analysis is conducted for priority-based distributed systems and the synthesis problem is partially addressed by using genetic algorithms for optimizing priority and period assignments. In [7], task allocation and priority assignment are explored to optimize a metric of extensibility in which all task times are scaled by a constant factor. In [8], a general definition of extensibility at the task level is presented and a genetic algorithm is proposed.

In our previous work [12][13], we optimize a task extensibility metric that measures how much the execution times of software tasks can be increased without violating schedulability constraints, through exploration of task and message allocation and scheduling. We demonstrate that we may achieve 30-40% improvement on the task-level extensibility metric with respect to the initial design from industry. More recently in [14], we study extensibility for functional models with finite state machine (FSM) semantics, and define an action extensibility metric. We propose an algorithm that optimizes this metric through multi-task generation of FSMs and is able to provide a 20-150% improvement.

Improving extensibility for cyber-physical systems is a critical and challenging area. The works above have only addressed the tip of the iceberg. This is an urgent need for new methodologies and tools to design extensible systems and efficiently validate software and hardware updates.

Reference

Updates

A. AWARDS for 2016

1. Awards of iNIS 2016:

**IEEE TCVLSI TRAVEL GRANT RECIPIENTS**
1. Venkata P. Yanambaka - PhD Scholar (University of North Texas)
2. Raj Mani Shukla – PhD Scholar (University of Nevada, Reno, USA)
3. Rituraj S. Rathore – PhD Scholar (NIT, Hamirpur, INDIA)
4. Akash Saini – B.Tech Student (NSIT, New Delhi, INDIA)

**BEST RESEARCH PAPER AWARDEES**

- **a. Best Paper award with cash prize:**
  1) Paper Name - Width-Dependent Characteristics of Graphene Nanoribbon Field Effect Transistor for High Frequency Applications. Awardees - Yaser M. Banadaki and Ashok Srivastava. (Louisiana State University, LA, USA)

- **b. Best Paper award without cash prize:**
  1) Paper Name - Computing in Ribosomes: Implementing Sequential Circuits using mRNA-Ribosome System . Awardees - Pratima Chatterjee, Mayukh Sarkar and Prasun Ghosal (IIEST, Shibpur, INDIA)

2. The best paper award of ACSD 2016 was awarded to this paper:

Raymond Devillers: Products of Transition Systems and Additions of Petri Nets

3. The best paper award for ASYNC 2016 went to:

Ring Oscillator Clocks and Margins
Jordi Cortadella, Marc Lupon, Alberto Moreno, Antoni Roca and Sachin Sapatnekar

4. TCVLSI Student Travel Awards at SLIP 2106:
  a. Mohammad Ahmed mahmed@pdx.edu Portland State University
  b. Scott Lerner spI29@drexel.edu Drexel University

5. The Best Paper Award winner of SLIP’16 is as follows:

Best Student Paper Award:

6. Following ISVLSI 2016 awards:

2 student travel awards:
Maria Malik, George Mason University, USA
Sunil Kumar Maddikatla, IIIT Hyderabad, India

Following are the paper awards:
TCVLSI best paper award:
Sunil Kumar Maddikatla and Srivatsava Jandhyala: An Accurate CMOS Integrated Temperature Sensor For IOT Applications

Amar Mukherjee Best Paper Award:
Innocent Agbo, Mottaqiallah Taouil, Said Hamdioui, Pieter Weckx, Stefan Cosemans, Praveen Raghavan, Francky Catthoor and Wim Dehaene: Quantification of Sense Amplifier Offset Voltage Degradation due to Zero- and Run-time Variability

Best Poster Award:
Jaya Dofe, Yuejun Zhang and Qiaoyan Yu: DSD: A Dynamic State-Deflection Method for Gate-Level Netlist Obfuscation

B. AWARDS for 2017

TCVLSI announces multiple students travels awards and best paper awards for 2017. Author and student attendees are encouraged to contact respective conference chairs for more information. TCVLSI announces one award each of $150 for ARITH 2017, ASAP 2017, ASYNC 2017, ECMSM 2017, iNIS 2017, ISVLSI 2017, IWLS 2017, MSE 2017, SLIP 2017. TCVLSI also announces multiple students travels awards as follows:

<table>
<thead>
<tr>
<th>Quantity</th>
<th>Conference Name</th>
<th>Amount per Award</th>
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<tbody>
<tr>
<td>3</td>
<td>ARITH 2017</td>
<td>$250.00</td>
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<tr>
<td>3</td>
<td>ASAP 2017</td>
<td>$250.00</td>
</tr>
<tr>
<td>3</td>
<td>ASYNC 2017</td>
<td>$250.00</td>
</tr>
<tr>
<td>1</td>
<td>ECMSM 2017</td>
<td>$250.00</td>
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<tr>
<td>3</td>
<td>iNIS 2017</td>
<td>$250.00</td>
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<tr>
<td>3</td>
<td>ISVLSI 2017</td>
<td>$250.00</td>
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<tr>
<td>2</td>
<td>IWLS 2017</td>
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<td>2</td>
<td>MSE 2017</td>
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<tr>
<td>2</td>
<td>SLIP 2017</td>
<td>$250.00</td>
</tr>
</tbody>
</table>

C. CALL FOR PAPERS (CFPs)

************************************************************************************
IEEE COMPUTER SOCIETY ANNUAL SYMPOSIUM ON VLSI July 3-5, 2017, Bochum, Germany
http://www.isvlsi.org

The submission interface is open for contributions to the IEEE COMPUTER SOCIETY ANNUAL SYMPOSIUM ON VLSI which is held from July 3-5th in Bochum Germany.

We already have 3 confirmed keynotes:
* Mr. Jens Werner, Vice President Cadence, Field Engineering EMEA
* Prof. Pierre-Emmanuel Gaillardon, from the University of Utah
* Prof. Georges Gielen, Vice Rector of KU Leuven for the Group Science, Technology & Engineering, Belgium

The symposium will have a strong industrial support with an exhibition, side events, talks etc.

Besides the excellent scientific content, also the social event will be a highlight during the conference:
* The welcome Reception in a cinema in Bochum's city with the talk "Shaken, not stirred! James Bond in the Focus of Physics" from Prof. Metin Tolan, University Dortmund is held before the attendees can see a nice James Bond movie with popcorn and drinks.
* The main social event with dinner is on a boat and during the trip we will have a "magic" entertainment on board with a well-known magician.

The Symposium explores emerging trends and novel ideas and concepts covering a broad range of topics in the area of VLSI: from VLSI circuits, systems and design methods, to system level design and system-on-chip issues, to bringing VLSI methods to new areas and technologies like nano- and molecular devices, MEMS, and quantum computing. Future design methodologies are also one of the key topics at the Symposium, as well as new EDA tools to support them. Over three decades the Symposium has been a unique forum promoting multidisciplinary research and new visionary approaches in the area of VLSI, bringing together leading scientists and researchers from academia and industry.

The Symposium Proceedings are published by IEEE Computer Society Press. Papers from past ISVLSI editions have been subsequently published in special issues of top archival journals which indicates the general high quality of the papers. The Symposium has established a reputation in bringing together well-known international scientists as invited speakers; the emphasis on high quality will continue at this and future editions of the Symposium.

Contributions are sought in the following areas:


The Symposium Program will include contributed papers and speakers invited by the Program Committee, as well as a poster session. Keynote addresses, panels and special sessions are planned as well. Authors should submit their original work using the web based submission system. Initial submissions to the conference are limited to six pages. All submissions should be in PDF format.

**Important dates are:**

Submission Deadline: February 24, 2017

Acceptance Notification: April 15, 2017

Submission of Final Version: May 12, 2017

Selected papers from ISVLSI 2017 will be invited for submission to a journal special issue. The selection process is based on reviewer feedback and quality of conference presentation.

**Organizing Committee**

**General Chairs**
Michael Hubner  
Ruhr-University of Bochum, Germany  
Michael.Huebner@ruhr-uni-bochum.de

Ricardo Reis  
UFRGS, Brazil  
reis@inf.ufrgs.br

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Nikos Voros  
Technological Educational Institute of Western Greece, Greece

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Nils Pohl, RUB, Germany
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Horst Gass, RUB, Germany

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Susmita Sur-Kolay, Indian Statistical Institute, Kolkata, India
Vijaykrishnan Narayanan, Pennsylvanian State University, USA

All information is available on [www.isvlsi.org](http://www.isvlsi.org)

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**IEEE iNIS 2017 - DEADLINE: July 2, 2017 - CFP**

3rd IEEE INTERNATIONAL SYMPOSIUM ON NANOELECTRONIC AND INFORMATION SYSTEMS

December 18-20, 2017, Bhopal, India.

http://www.ieee-inis.org

The primary objective of IEEE-iNIS 2017 is to provide a platform for both hardware and software researchers to interact under one umbrella for further development of efficient and secure information processing technologies. Efficient and secure data sensing, storage, and processing play pivotal roles in current information age. The state-of-
the-art nanoelectronic technology based hardware systems cater to the needs of efficient sensing, storage, and computing. At the same time, efficient algorithms and software used for faster analysis and retrieval of desired information are becoming increasingly important. Big data which are large, complex data sets, are now a part of the Internet world. Storing and processing needs of the enormous amount of structured and unstructured data are getting increasingly challenging. At the same time, Internet of Things (IoT) and cyber-physical systems (CPS) have been evolving with simultaneous development of hardware and software and span across everyday consumer electronics. The performance and efficiency of the present as well as the future generations of computing and information processing systems are largely dependent upon advances in both hardware and software.

iNIS 2017 is sponsored by IEEE-CS under TCVLSI and technically co-sponsored by IEEE-CAS as well as IEEE-CEDA. iNIS has been initiated as a sponsored meeting of Technical Committee on VLSI, IEEE-CS (http://www.ieee-tcvlsi.org/) that endorses a league of successful meetings such as ASAP, ISVLSI, ARITH, etc., which are now presented as "Sister Conferences" in the iNIS website. iNIS brings together leading scientists and researchers from academia and industry.

Contributions are sought in (but are not limited to) the following areas:
(1) Nanoelectronic VLSI and Sensor Systems (NVS)
(2) Energy-Efficient, Reliable VLSI Systems (ERS)
(3) Hardware/Software for Internet of Things (IOT) and Consumer Electronics (CE)
(4) Hardware for Secure Information Processing (SIP)
(5) Hardware/Software Solutions for Big Data (SBD)
(6) Cyber Physical Systems and Social Networks (CSN)

Detailed description of the tracks is provided in the iNIS website.

iNIS 2017 proceedings will be published by IEEE-CS conference publication services (CPS). Authors are invited to submit full-length (6 pages maximum), original, unpublished research papers with an abstract (200 words maximum). To enable blind review, the author list should be omitted from the main document. Papers violating length and blind-review criteria would be excluded from the review process. Previously published papers or papers currently under review for other conferences/journals should not be submitted and will not be considered for publication. Authors should submit their original work of maximum 6 pages using double-column IEEE-CS conference format-template (http://www.ieee.org/conferences_events/conferences/publishing/templates.html). A selected papers from iNIS 2017 program will be invited for submission to a peer-reviewed journal special issue based on reviewer feedback and quality of conference presentation.

Paper Submission Site:
https://easychair.org/conferences/?conf=inis2017

Important dates of iNIS 2017 are the following:

Submission Deadline: July 2, 2017
Acceptance Notification: September 15, 2017
Submission of Final Version: October 10, 2017

Special Sessions and Panels: iNIS 2017 will consider proposals for special sessions as well as panels. Special session and panel proposals can be submitted to the special session chairs by email: hthapliyal@uky.edu and hai.li@duke.edu. The submission deadline is the same as specified for the regular paper submissions.

Student Research Symposium: iNIS 2017 will host a student research symposium. A single 2-page pdf file for student research symposium paper can be submitted to the student symposium chairs by email: sunilsingh@oriental.ac.in. The submission deadline is the same as specified for the regular paper submissions. All the accepted student research symposium papers will be published in the conference souvenir. A selected top 5 of these will be published in the iNIS 2017 proceedings.
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Prasun Ghosal, IIEST, India

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Anirban Sengupta, Indian Institute of Technology (I.I.T) Indore
Jawar Singh, IIITDM, Jabalpur

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Saumya Kanti Datta, Eurecom, France

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Taruna Jain, Barkatullah UIT, Bhopal, India
Deepak Verma, MANIT, Bhopal, India

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Sunil Singh, OIST, Bhopal, India

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Rahul Dubey, OIST, Bhopal, India
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Nagi Naganathan, Avago Technologies, USA
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Dhruva Ghai, Oriental University, India, Vice Chair
Aida Todri-Sanial, CNRS-LIRMM, France
Ashok Srivastava, Louisiana State University, USA
Hai (Helen) Li, University of Pittsburgh, USA
ARITH 24:

Since 1969, the ARITH symposia have served as the flagship conference for presenting scientific work on the latest research in computer arithmetic. Authors are invited to submit papers describing recent advances on all aspects of computer arithmetic and its applications or implementations. This includes, but is not restricted to, the following topics:

1) Foundations of number systems and arithmetic
2) Arithmetic processor design and implementation
3) Arithmetic algorithms and their analysis
4) Floating-point units, algorithms, and numerical analysis
5) Elementary and special function implementations
6) Power-efficient or low-energy arithmetic units and processors
7) Industrial implementation of arithmetic units and processors
8) Test, validation, and formal verification techniques for arithmetic implementations
9) Fault/error-tolerance in arithmetic implementations
10) Arithmetic for FPGAs and reconfigurable logic
11) Design automation for computer arithmetic implementations
12) Computer arithmetic for security and cryptography
13) Arithmetic to enhance accuracy or reliability (multiple-precision, interval arithmetic, ...)
14) Arithmetic challenges in HPC and exascale computing (accuracy, reproducibility, ...)
15) Arithmetic for specific application domains (big-data analytics, signal processing, computer graphics, multimedia, computer vision, finance, ...)
16) Computer arithmetic in emerging technologies
17) Non-conventional computer arithmetic and applications

Procedure for submission

A PDF version of the full paper should be submitted no later than Jan 31st (Final deadline), 2017. Papers under review elsewhere are not acceptable for submission to ARITH 24. By submitting a paper you implicitly confirm you are solely submitting it to ARITH 24. Authors will be notified of acceptance in March 2017, and final camera-ready papers will be due in May 2017.

Submission site: https://easychair.org/conferences/?conf=arith24

Note on paper formatting

The final submissions of accepted papers cannot exceed 8 pages (NO extra pages) using the IEEE Computer Society Conference format (two columns). However, for review, authors may submit a paper with a maximum of 20 pages, 12pt font size, single column and double spacing.

Formatting instructions: http://www.ieee.org/conferences_events/conferences/publishing/templates.html

ASAP 2017

The 28th International IEEE Conference on Application-specific Systems, Architectures and Processors
Seattle, Washington USA, Seattle Grand Hyatt
July 10th-12th 2017
www.asapconference.org

The ASAP 2017 conference will cover the theory and practice of application-specific systems, architectures and processors. We will build upon traditional strengths of the conference in areas such as computer arithmetic, cryptography,
compression, signal and image processing, network processing, reconfigurable computing, and all types of hardware accelerators. We especially encourage submissions in the following areas:

1) Big data analytics: extracting and correlating information from large-scale semi-structured and unstructured data using application-specific systems.
2) Machine learning: specialized platforms or hardware-optimized algorithms to improve the performance or efficiency of model creation and/or prediction.
3) Scientific computing: architectures and algorithms that address scientific applications requiring significant computing power and design customization (bioinformatics, climate modeling, astrophysics, seismology, etc.).
4) Industrial computing: systems and architectures for providing high-throughput or low latency in various industrial computing applications.
5) System security: cryptographic hardware architectures, security processors, countermeasures against side-channel attacks, and secure cloud computing.
6) Heterogeneous systems: applications and platforms that exploit heterogeneous computing resources, including FPGAs, GPUs, or CGRAs.
7) Design space exploration: methods for customizing and tuning application-specific architectures to improve efficiency and productivity.
8) Platform-specific architectures: novel architectures for exploiting specific compute domains such as smartphones, tablets, and data centers, particularly in the context of energy efficiency.

ASAP 2017 will accept 8-page full papers for oral presentations and 4-page short papers for short oral or poster presentations, with a double-blind review process. Manuscripts must not identify authors or their affiliations. An online submission page will be made available on the website and will include detailed guidelines and links to formatting templates.

Important Dates:
Submissions Due: April 3
Author Notification: May 12
Camera Ready Due: June 2
Early Registration Ends: June 2
Conference: July 10 to 12

ASYNC 2017:

Regular Papers
Authors are invited to submit papers on any aspect of synchronous design topics ranging from design, synthesis, and test, to asynchronous applications in system-level integration and emerging computing technologies. Topics of interest include:
1) Mixed-timed circuits, GALS systems, networks-on-chips, multi-chip interconnects, and 3D integration;
2) Elastic and latency-tolerant synchronous design;
3) Asynchronous pipelines, architectures, CPUs, and memories;
4) Asynchronous logic in ultra-low power and power-constrained systems, energy harvesting and mixed-signal/analog design;
5) Asynchrony in emerging technologies, including bio, neural, nano, and quantum computing;
6) CAD tools for asynchronous design, synthesis, analysis, and optimization;
7) Formal methods for verification and performance/power analysis;
8) Test, security, fault tolerance, and radiation-hard design;
9) Asynchronous variability-tolerant, resilient design and design for manufacturing;
10) Asynchronous design for neural networks and machine learning applications;
11) Circuit designs, case studies, comparisons, and applications.

Submissions must report original scientific work, in 6-8 pages IEEE double-column conference format, with author information concealed. Accepted papers will be published in the IEEE digital library IEEEExplore and symposium proceedings.

Industrial Papers
ASYNC 2017 will include a special industrial workshop with papers and tutorials from industry on the state-of-the-art application of asynchronous designs to both existing and emerging technologies. The topics are specifically targeted at industry and include:
1) Synchronizers and clock domain crossing techniques;
2) Techniques for combining asynchronous and clocked designs;
3) CAD tools for integrating asynchronous circuits with clocked designs;
4) Circuit designs, case studies, comparisons, and applications.

We solicit 1-page to 2-page submissions for the workshop, IEEE double-column conference format. These papers will go through a separate light-weight review process. Accepted papers will be published in the IEEE digital library IEEEXplore and symposium proceedings.

**Fresh Ideas Workshop**
ASYNC 2017 will accommodate a special workshop to present “fresh ideas” in asynchronous design, that are not yet ready for publication. We solicit 1-to-2-page submissions for the workshop, which will go through a separate light-weight review process. Accepted submissions will be handed out at the workshop.

**Important Dates**
Regular Track Abstract Registration Deadline: December 2, 2016? November 25, 2016?
Regular Track Full Paper Submission Deadline: December 16, 2016? December 2, 2016?
Regular Track Notification of Acceptance: February 10, 2017
Fresh Ideas Workshop Submission Deadline: February 24, 2017
Industrial Papers Submission Deadline: February 24, 2017
Publication-Ready Final Version: March 10, 2017

*IWLS 2017*

**The 26th International Workshop on Logic & Synthesis**
June 17 – June 18, 2017
Thompson Conference Center – Austin, TX
www.iwls.org

Sponsored by, The International Workshop on Logic and Synthesis is the premier forum for research in synthesis, optimization, and verification of integrated circuits ans systems. Research on logic synthesis for emerging technologies and for novel computing platforms, such as nanoscale systems and biological systems, is also strongly encouraged. The workshop encourages early dissemination of ideas and results. The workshop accepts complete papers highlighting important new problems in the early stages of development, without providing complete solutions. The emphasis is on novelty and intellectual rigor. Topics of interest include, but are not limited to: hardware synthesis and optimization; software synthesis; hardware/software co-synthesis; power and timing analysis; testing, validation and verification; synthesis for reconfigurable architectures; hardware compilation for domain-specific languages; and design experiences. Submissions on modeling, analysis and synthesis for emerging technologies and platforms are particularly encouraged. Only complete papers with original and previously unpublished material are permitted. Submissions must be no longer than 8 pages, double column, 10-point font. Accepted papers are distributed only to IWLS participants. The workshop format includes paper presentations, posters, invited talks, social lunch and dinner gatherings, and recreational activities. Submissions are made electronically through EasyChair. Please see the workshop website for instructions: http://www.iwls.org. You must register the paper by submitting an abstract before the deadline below.

Paper abstract submission: March 5, 2017
Full paper submission: March 12, 2017 - 11.59pm Anywhere on Earth
Notification of acceptance: April 16, 2017
Final version due: May 14, 2017

The submission deadline is final and there will be no extensions. In 2017, the IWLS organizing committee set up a programming contest. To participate, please refer to the workshop website (http://www.iwls.org).

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K.-C. Wu, National Chiao Tung University, ROC
MSE 2017:

The IEEE Computer Society International Conference on Microelectronic Systems Education is the premier conference dedicated to furthering undergraduate and graduate education in designing and building innovative microelectronics systems. The conference is held in the U.S. in odd years, and in Europe in even years, when it is called the European Workshop on Microelectronics Education (EWME). MSE is a single track conference with an interactive poster session, providing each paper excellent exposure. The poster session encourages demonstrations and hands-on experiences for the attendants to encourage rich discussions. Co-located with the Great Lakes Symposium on VLSI (GLSVLSI), participants will be provided with a unique opportunity to attend both conferences. This combination of a technical and an educational conference allows attendants to see what technologies are on the horizon and discuss how they can be taught effectively in the classroom. Topics of Interest The MSE conference provides an excellent opportunity for educators and industry to work together to ensure continued excellence in the field of microelectronic systems. Of particular interest is incorporation of emerging trends in the microelectronic system industry and research into the classroom.

Papers are invited in (but not limited to) the following areas:
- Pedagogical innovations using a wide range of technologies, including nanometer-scale integrated circuits, low-power design, nanotechnology, application-specific integrated circuits (ASICs), field programmable gate arrays (FPGAs), multicore/many-core processors, graphics processing units (GPUs), sensor networks, and embedded systems.
- Educational techniques including novel curricula and laboratories, assessment methods, distance learning, textbooks, and design projects.
- Industry and academic collaborative programs and teaching.
- Preparing students for industry, entrepreneurship, academics, and/or research.

Submission MSE 2017 welcomes two paper submission types: Full papers should not exceed four (4) pages in length. Work In Progress papers should be limited to two (2) pages in length and should be used to present work in an intermediate stage, perhaps not fully assessed, for which the authors would like to strike a conversation with the community. All submissions must comply with IEEE Computer Society formatting requirements. Submissions in PDF or postscript format may be submitted on-line at www.mseconference.org. Submissions will be judged on originality, appropriateness, technical strength, assessment, and other relevant criteria.

Important Dates
Submission of papers: January 30, 2017
Notification of acceptance March 6, 2017
Submission of final papers March 22, 2017

General Chair
Ozcan Ozturk
Bilkent University
Ozturk@cs.bilkent.edu.tr

Program Chair
Tina Hudson
Rose-Hulman Institute of Technology
hudson@rose-hulman.edu

SLIP 2017

June 17, 2017, Austin Convention Center, Austin, TX, USA

The general technical scope of the workshop is the design, analysis, prediction, and optimization of interconnect and communication fabrics in electronic systems. The organizing committee invites original contributions to the workshop. These contributions include papers, tutorials, panels, special sessions, and posters. We accept papers based on novelty and
contributions to the advancement of the field. The accepted papers will be published in the ACM and IEEE digital libraries. Technical topics include but are not limited to:

- Interconnect prediction and optimization at various IC and system design stages
- System-level design for FPGAs, NOCs, reconfigurable systems
- Design, analysis, and optimization of power and clock networks
- Interconnect reliability
- Interconnect topologies and fabrics of multi- and many-core architectures
- Design-for-manufacturing (DFM) and yield techniques for interconnects
- High speed chip-to-chip interconnect design
- Design and analysis of chip package interfaces
- Power consumption of interconnects
- 3D interconnect design and prediction
- Emerging interconnect technologies
- Applications of interconnects to social, genetic, and biological systems
- Co-optimization of interconnect technology and chip design

Submission:
We invite authors to submit papers of 4 to 8 pages, double-columned, 9pt or 10pt font in ACM proceedings format available at www.acm.org/sigs/publications/proceedings-templates

To permit double blind review, all papers must remove author information (submissions with author information will be rejected). Authors should submit papers electronically: http://www.easychair.org/conferences/?conf=slip2017

(New) Student Awards:
Provided by the IEEE Computer Society’s Technical Committee on VLSI (TCVLSI), the Best Student Paper Award will be awarded for a SLIP2017 paper whose first author is a student. In addition, limited student travel grants of $250 are available. Details will follow on the website.

Format:
The workshop includes keynotes, regular paper sessions, interactive panels, tutorials, invited talks, and interactive poster sessions. Our program also includes lunch, refreshments, and a traditional social dinner with fun elements.

Important Dates:
Abstract Registration: Mar 11, 2017
Paper Submission: Mar 18, 2017
Author Notification: April 22, 2017
Final Version Upload: May 1, 2017

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17th International Conference on Application of Concurrency to System Design (ACSD 2017)
Zaragoza, Spain, June 25-30, 2017
http://pn2017.unizar.es/

The 17th International Conference on Application of Concurrency to System Design (ACSD 2017) will be organized by the Aragón Institute of Engineering Research (I3A), of Zaragoza University, Zaragoza, Spain. The conference will take place at the School of Engineering and Architecture (EINA) of Zaragoza University. The language of the conference is English. The conference aims at cross-fertilizing both theoretical and applied research about formal approaches (in a broad sense) to designing computer systems that exhibit some kind of concurrent behaviour. In particular, the following topics are of interest:

1) Formal models of computation and concurrency for the above systems and problems, like data-flow models, communicating automata, Petri nets, process algebras, graph rewriting systems, state charts, MSCs, modal and temporal logics
2) Compositional design principles like modular synthesis, distributed simulation and implementation, distributed control, adaptivity, supervisory control
3) Algorithms and tools for concurrent systems, ranging from programming languages to algorithmic methods for system analysis and construction, including model checking, verification, and static analysis techniques as well as synthesis procedures
4) Synchronous and asynchronous systems on all design levels: polychronous systems, endochronous systems, globally asynchronous locally synchronous systems

5) Cyber-physical systems, hybrid systems, networked systems, and networks in biological systems

6) High-performance computer architectures like many-core processors, networks on chip, graphics processing units, instruction-level parallelism, dataflow architectures, up to ad-hoc, mobile, and wireless networks

7) Memory consistency models for multiprocessor and multicore architectures, replicated data, including software and hardware memory models, DRAM scheduling, cache coherency, memory-aware algorithms Real-time aspects, including hard real-time requirements, security and safety-critical issues, functional and timing verification

8) Implementation aspects like resource management, including task and communication scheduling, network-, memory-, and power-management, energy/power distribution, fault-tolerance, quality of service, scalability, load balancing, power proportionality

9) Design principles for concurrent systems, in particular hardware/software co-design, platform-based design, component-based design, energy-aware design, refinement techniques, hardware/software abstractions, cross-layer optimization

10) Business process modelling, workflow execution systems, process (de-)composition, inter-organizational and heterogeneous workflow systems, systems for computer-supported collaborative work, web services

11) Case studies of general interest, from industrial applications to consumer electronics and multimedia, automotive systems, (bio-)medical applications, neuromorphic applications, internet (of things) and grid computing, to gaming applications.

Paper Submission

ACSD seeks papers describing original work which has not been previously published and is not under review for publication elsewhere. All files must be prepared using the latest IEEE Computer Society conference proceedings guidelines (8.5” x 11” two-column format). The page limit for regular papers is 10 pages.

In addition to regular submissions, there will be a tools section. Tools will be presented at the conference in an interactive session. Related papers describe a tool, its functionality and interfaces as well as the underlying algorithms and implementation aspects. These tool papers are limited to 6 pages.

Conference proceedings will be submitted for inclusion to IEEE Xplore. Accepted regular and tool papers will be included in the conference proceedings. At least one authors of each accepted contribution is expected to present the paper or tool at the conference, and will be required to sign the copyright release forms.

Several papers will be considered for publication in extended and revised form in a special issue of a journal.

STEERING COMMITTEE
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Jörg Desel, Germany

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36th IEEE INTERNATIONAL CONFERENCE ON CONSUMER ELECTRONICS (ICCE)

The IEEE Consumer Electronics (CE) Society is soliciting technical papers for oral and poster presentations at their 36th annual conference, IEEE International Conference on Consumer Electronics (ICCE) in Las Vegas. ICCE is the established forum for innovative research in all areas of consumer electronics. The theme of ICCE 2018 is “Cybersecurity”.

Contributions are sought in but are not limited to following areas:
(1) Security and Privacy of CE Hardware & Software Systems (SPC)
(2) Energy Management of CE Hardware & Software Systems (EMC)
(3) Application-Specific CE for Smart Cities (SMC)
(4) Wireless, Network Technologies and its Security (WNT)
(5) Internet of Things (IoT) & its Security
(6) Entertainment, Gaming, Virtual & Augmented Reality (EGV)
In addition to regular oral and poster sessions based on the above tracks, ICCE 2018 will have many special sessions on current hot topics. ICCE 2018 will also have industry tracks. ICC 2018 will have a **student research forum** as its integral part. ICCE 2018 invites **proposals for special sessions, industry tracks, and expert panels.**

Authors are invited to submit original and unpublished research manuscripts with an abstract (200 words) and 2- to 6-page length. Previously published papers or papers currently under review for other conferences/journals should not be submitted and will not be considered for publication. Authors should submit their original work of maximum 6 pages using double-column IEEE conference format-template ([http://www.ieee.org/conferences_events/conferences/publishing/templates.html](http://www.ieee.org/conferences_events/conferences/publishing/templates.html)). All accepted papers will be published in the ICCE Digest and submitted to IEEE Xplore. Instructions for authors and document templates are available on the conference website. A selected set of papers from ICCE 2018 program will be invited for submission to special issues of peer-reviewed journals (e.g. CE Magazine/Transactions) based on reviewer’s feedback and quality of conference presentation. This year features Special Sessions/Tutorials on Cybersecurity.

Important dates of ICCE 2018 are the following:

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**Submission Deadline:** July 15, 2017  |  **Acceptance Notification:** September 15, 2017  |  **Submission of Final Version:** October 15, 2017

**ICCE 2018 Organizing Committee:**
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**General Chair:**
Saraju P. Mohanty, University of North Texas, USA

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Peter Corcoran, National University of Ireland Galway, Ireland
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**Program Chairs:**
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Industry Liaison Chairs:
L. Dennis Shapiro, Arzak Corporation, USA
Stephen Dukes, Imaginary Universes LLC, USA

Conference Coordinator:
Charlotte Kobert, CESoc staff, USA
Outreach and Community

Have you led or participated in outreach related to your research?

Would you like to be featured in an upcoming issue of VLSI Circuits and Systems Letter?

Send an email to mike.borowczak@uwyo.edu with your contact information, any details and/or pictures from your outreach event and well follow up with you!
Call for Contributions

The VLSI Circuits and Systems Letter aims to provide timely updates on technologies, educations and opportunities related to VLSI circuits and systems for TCVLSI members. The letter will be published twice a year and it contains the following sections:

- **Features**: selective short papers within the technical scope of TCVLSI, “What is” section to introduce interesting topics related to TCVLSI, and short review/survey papers on emerging topics in the areas of VLSI circuits and systems.
- **Opinions**: Discussions and book reviews on recent VLSI/nanoelectronic/emerging circuits and systems for nano computing, and “Expert Talks” to include the interviews of eminent experts for their concerns and predictions on cutting-edge technologies.
- **Updates**: Upcoming conferences/workshops of interest to TCVLSI members, call for papers of conferences and journals for TCVLSI members, funding opportunities and job openings in academia or industry relevant to TCVLSI members, and TCVLSI member news.
- **Outreach and Community**: The “Outreach K20” section highlights integrating VLSI computing concepts with activities for K-4, 4-8, 9-12 and/or undergraduate students. It also features student fellowship information as well a “Puzzle” section for our readership.

We are soliciting contributions to all these four sections. Please directly contact the editors and/or associate editors by email to submit your contributions.

**Submission Deadline:**
All contributions must be submitted by May 7, 2017 in order to be included in the June issue of the letter.

**Editors:**
- Saraju Mohanty, University of North Texas, USA, saraju.mohanty@unt.edu
- Xin Li, Duke University, USA, xinli.ece@duke.edu

**Associate Editors:**
- **Executive**: Yiyu Shi, University of Notre Dame, USA, yshi4@nd.edu
- **Features**: Shiyan Hu, Michigan Technological University, USA, shiyan@mtu.edu
- **Features**: Saket Srivastava, University of Lincoln, United Kingdom, ssrivastava@lincoln.ac.uk
- **Features**: Qi Zhu, University of California, Riverside, USA, qzhu@ece.ucr.edu
- **Opinions**: Prasun Ghosal, Indian Institute of Engineering Science and Technology, India, p_ghosal@it.iests.ac.in
- **Opinions**: Michael Hübner, Ruhr-University of Bochum, Germany, Michael.Huebner@ruhr-uni-bochum.de
- **Opinions**: Jawar Singh, Indian Institute of Information Technology, Design and Manufacturing, Jabalpur, India, jawar@iiitdmj.ac.in
- **Updates**: Helen Li, University of Pittsburg, USA, hal66@pitt.edu
- **Updates**: Anirban Sengupta, Indian Institute of Technology, Indore, India, asengupt@iiti.ac.in
- **Updates**: Jun Tao, Fudan University, China, taojun@fudan.edu.cn
- **Outreach and Community**: Mike Borowczak, University of Wyoming, USA, mborowcz@uwyo.edu
Editorial Board

Saraju P. Mohanty is a Professor at the Department of Computer Science and Engineering (CSE), University of North Texas (UNT), where he directs the NanoSystem Design Laboratory (NSDL). He obtained a Ph.D. in Computer Engineering from the University of South Florida (USF) in 2003, a Master’s degree in Systems Science and Automation (SSA) from the Indian Institute of Science (IISc), Bangalore, India in 1999, and a Bachelor’s degree (Honors) in Electrical Engineering from Orissa University of Agriculture and Technology (OUAT), Bhubaneswar, India in 1995. Prof. Mohanty’s research is in “Energy-Efficient High-Performance Secure Electronic Systems”. Prof. Mohanty’s research has been funded by National Science Foundation (NSF), Semiconductor Research Corporation (SRC), and Air Force. Dr. Mohanty is an inventor of 4 US patents. Prof. Mohanty is an author of 220 peer-reviewed journal and conference articles, and 3 books. The publications are well-received by the world-wide peers with a total of 2900 citations leading to an h-index of 27 and i10-index of 75 (from Google Scholar). His latest book titled Nanoelectronic Mixed-Signal System Design is published by McGraw-Hill in 2015 is a best seller. This book received 2016 PROSE Award for best Textbook in Physical Sciences & Mathematics from the Association of American Publishers. He received 2016-17 UNT Toulouse Scholars Award for sustained excellent teaching and scholarly achievements. Prof. Mohanty has been serving on the editorial board of several peer-reviewed international journals or transactions. He currently serves on the editorial board of 6 peer-reviewed international journals, including IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), ACM Journal on Emerging Technologies in Computing Systems (JETC), and IET Circuits, Devices & Systems Journal (CDS). He is currently the Editor-in-Chief (EiC) of the IEEE Consumer Electronics Magazine. He serves as a founding Editor-in-Chief (EiC) of the VLSI Circuits and Systems Letter (VCAL). He has been serving as a guest editor for many prestigious journals including ACM Journal on Emerging Technologies in Computing Systems (JETC) and IEEE Transactions on Emerging Topics in Computing (TETC). Prof. Mohanty currently serves as the Chair of Technical Committee on Very Large Scale Integration (TCVLSI), IEEE Computer Society (IEEE-CS) to oversee a dozen of IEEE conferences. He serves on the steering, organizing, and program committees of several international conferences. He is the founding steering committee chair for the IEEE International Symposium on Nanoelectronic and Information Systems (iNIS) and steering committee vice-chair of the IEEE-CS Symposium on VLSI (ISVLSI). Prof. Mohanty is a senior member of IEEE and ACM. Prof. Mohanty has supervised 8 Ph.D. dissertations and 25 M.S. theses; eight of these advisees have received outstanding student awards at UNT. He has received Honors Day recognition as an inspirational faculty at the UNT for multiple years. He has also received UNT Provost’s Thank a Teacher recognition for multiple years. More about his biography, research, education, and outreach activities can be obtained from his website: http://www.smohanty.org.

Xin Li is currently a Professor in the Department of Electrical and Computer Engineering, Duke University, Durham, NC. In 2005, he co-founded Xigmix Inc. to commercialize his PhD research, and served as the Chief Technical Officer until the company was acquired by Extreme DA in 2007. In 2011, Extreme DA was further acquired by Synopsis (Nasdaq: SNPS). From 2009 to 2012, he was the Assistant Director for FCRP Focus Research Center for Circuit & System Solutions (C2S2), a national consortium of 13 research universities (CMU, MIT, Stanford, Berkeley, UIUC, UMich, Columbia, UCLA, among others) chartered by the U.S. semiconductor industry and U.S. Department of Defense to work on next-generation integrated circuit design challenges. From 2014 to 2015, he was the Assistant Director for the Center for Silicon System Implementation (CSSI), a CMU research center with 20 faculty members working on integrated circuits and systems. His research interests include integrated circuit, signal processing and data analytics. Dr. Xin Li was an Associate Editor of IEEE Trans. on Biomedical Engineering (TBME), IEEE Trans. on Computer-
Aided Design of Integrated Circuits and Systems (TCAD), ACM Trans. on Design Automation of Electronic Systems (TODAES), IEEE Design & Test (D&T), and Journal of Low Power Electronics (JOLPE). He was the Guest Editor for IEEE TCAD, IEEE TNANO, IEEE TBD, IEEE D&T, IEEE JETCAS, ACM TC, ACM JETC and VLSI Integration. He served on the Executive Committee of ACM Special Interest Group on Design Automation (SIGDA), IEEE Systems, Man, and Cybernetics Society Technical Committee on Cybernetics for Cyber-Physical Systems (TCCPS), and IEEE Computer Society Technical Committee on VLSI (TCVLSI). He was the General Chair of ISVLSI, iNIS and FAC, and the Technical Program Chair of CAD/Graphics. He also served on the ACM/SIGDA Outstanding PhD Dissertation Award Selection Committee, the IEEE TITC E. J. McCluskey Best Doctoral Thesis Selection Committee, the IEEE Outstanding Young Author Award Selection Committee, the Executive Committee of ISVLSI, GLSVLSI and iNIS, and the Technical Program Committee of DAC, ICCAD, ITC, ISVLSI, FAC, CAD/Graphics, ASICON and VLSI. He received the NSF Faculty Early Career Development Award (CAREER) in 2012, two IEEE Donald O. Pederson Best Paper Awards in 2013 and 2016, the Best Paper Award from Design Automation Conference (DAC) in 2010, two IEEE/ACM William J. McCalla ICCAD Best Paper Awards in 2004 and 2011, and the Best Paper Award from International Symposium on Integrated Circuits (ISIC) in 2014. In addition to these awards, he also received six Best Paper Nominations from Design Automation Conference (DAC), International Conference on Computer-Aided Design (ICCAD) and Custom Integrated Circuits Conference (CICC).

Dr. Yiyu Shi is currently an associate professor in the Department of Computer Science and Engineering and Electrical Engineering (concurrent appointment) at the University of Notre Dame. He received his B.S. degree (with honor) in Electronic Engineering from Tsinghua University, Beijing, China in 2005, the M.S and Ph.D. degree in Electrical Engineering from the University of California, Los Angeles in 2007 and 2009 respectively. He was an assistant professor in the Electrical and Computer Engineering Department at Missouri University of Science and Technology from 2010 to 2015, where he was the site founding co-director of the NSF I/UCRC Net-Centric Software and Systems Center. His current research interests include low-power design, three-dimensional integration, hardware security and renewable energy applications. In recognition of his research, eight of his papers have been nominated for the Best Paper Award and one paper have received the Best Paper in Track, all in top conferences (DAC'05, ICCAD'07, ICCD'08, ASPDAC'09, DAC'09, ISPD'13, ICCAD'14, ISPD'15, DAC'16). He was also the recipient of IBM Invention Achievement Award in 2009, Japan Society for the Promotion of Science (JSPS) Faculty Invitation Fellowship, Humboldt Research Fellowship, IEEE St. Louis Section Outstanding Educator Award, Academy of Science (St. Louis) Innovation Award, Missouri S&T Faculty Excellence Award, NSF CAREER Award, IEEE Region 5 Outstanding Individual Achievement Award, all in 2014, and the Air Force Summer Faculty Fellowship in 2015 and 2016. He has served on the technical program committee of many international conferences including DAC, ICCAD, DATE, ISPD, ASPDAC and ICCD. He is also a member of IEEE CEDA Publicity Committee and IEEE Smart Grid R&D Committee, and an associate editor of IEEE TCAD, ACM JETC, VLSI Integration, IEEE VLSI CAS Newsletter, IEEE TCCPS Newsletter and ACM SIGDA Newsletter. He is a senior member of IEEE.

Professor Shiyan Hu received his Ph.D. in Computer Engineering from Texas A&M University in 2008. He is an Associate Professor at Michigan Tech. where he is Director of Center for Cyber-Physical Systems and Associate Director of Institute of Computer and Cybersystems. He has been a Visiting Professor at IBM Research (Austin) in 2010, and a Visiting Associate Professor at Stanford University from 2015 to 2016. His research interests include Cyber-Physical Systems and Security, Data Analytics, and Computer-Aided Design of VLSI Circuits, where he has published more than 100 refereed papers. Prof. Hu is an ACM Distinguished Speaker, an IEEE Computer Society Distinguished Visitor, an invited participant for U.S. National Academy of Engineering Frontiers of Engineering Symposium, a recipient of National Science Foundation (NSF) CAREER Award, a recipient of ACM SIGDA Richard Newton DAC Scholarship (as the faculty advisor), and a recipient of JSPS Faculty Invitation Fellowship. Prof. Hu is the Chair for
Dr. Qi Zhu is an Assistant Professor at the Department of Electrical and Computer Engineering in University of California, Riverside. Prior to joining UCR, Dr. Zhu was a research scientist at the Strategic CAD Labs in Intel from 2008 to 2011. Dr. Zhu received a Ph.D. in EECS from University of California, Berkeley in 2008, and a B.E. in CS from Tsinghua University in 2003. His research interests include model-based design and software synthesis for cyber-physical systems, CPS security, energy-efficient buildings and infrastructures, and system-on-chip design. He received the National Science Foundation (NSF) CAREER award in 2016. He received best paper awards at the Design Automation Conference (DAC) 2006, DAC 2007, International Conference on Cyber-Physical Systems (ICCPS) 2013, and ACM Transactions on Design Automation of Electronic Systems (TODAES) 2016. Dr. Zhu has served on the technical program committees and as session organizer and chair for a number of international conferences, including DAC, ICCAD, DATE, ASP-DAC, CODES+ISSS, RTSS, RTAS, SAC, SIES, MEMOCODE, etc. He is a member and the education committee chair of the IEEE Technical Committee on Cybernetics for Cyber-Physical Systems (CCPS). He received the ACM SIGDA Service Award in 2015.

Jawar Singh is currently an Associate Professor in the Department of Electronics and Communication Engineering, PDPM-Indian Institute of Information Technology, Design and Manufacturing Jabalpur, MP, INDIA. He received Ph.D. degree from the University of Bristol, Bristol, UK. His research interest includes low power devices and circuits, and RF energy harvesting. Dr Singh holds two US patents related to static random access memories (SRAMs) and recipient of prestigious Indo-US fellowship BHAVAN 2016. His ongoing research is funded by Government of India (Department of Science and Technology, DST, and Ministry of Electronics and IT, Meity, New Delhi, INDIA). He was the visiting researcher of the Pennsylvania State University, USA and the University of North Texas, USA. Dr Singh is an Associate Editor of IET Electronics Letters and actively involved organizing various conference activities.

Dr. Prasun Ghosal is currently an Assistant Professor in the Department of Information Technology, Indian Institute of Engineering Science and Technology, Shibpur, India. He has been a visiting Assistant Professor in the Department of Computer Science and Engineering, University of North Texas, USA during 2013 - 2014 (under Raman Post Doctoral Fellowship from UGC, GOI) and a Heidelberg Laureate Post Doctoral Fellow (visited University of Heidelberg, Germany) in 2013. He received the PhD degree (Engg) from Bengal Engineering and Science University in 2011, M.Tech. and B.Tech. in Radio Physics and Electronics from Institute of Radio Physics and Electronics, University of Calcutta, India in 2005 and 2002 respectively, B.Sc. (Honours) in Physics in 1999 from University of Calcutta, India. His research is in Performance Centric, Power Aware Nanoscale Electronic System Design and Computing including Performance Centric Layout Design of 3D Integrated Circuits, Performance-centric, Power Aware Design of Networks-on-Chips (NoC), and Post Silicon Nanoscale Technologies and Computing viz. Memristors, DNA Computing, Reversible Circuit Synthesis etc. His research has been funded by AICTE, DIT, MCIT, Govt of India, IEI etc. He has contributed more than 90 research articles in several peer reviewed avenues of international journals and conferences. Besides a copyright he has also contributed towards several book chapters in edited volumes from different publishers including CRC press, and Springer-Verlag Berlin Heidelberg etc. He is a recipient of Young Scientist Research Award 2011 from Indian Science Congress Association, recipient of several Best Paper Awards in IEEE iNIS 2016, ICFAE - 2014 from IEEE CS, ADCONS - 2011 etc., Best Paper Award Nominee in ISVLSI - 2008. He is the Vice Chair of the Steering Committee and one
of the Founding member of IEEE iNIS (IEEE International Symposium on Nanoelectronic and Information Systems). He has served/is serving as General/Program Chair/Track Chair/TPC member in several conference committees including IEEE/ACM GLSVLSI, ISVLSI, IEEE iNIS, ACM MobiHoc, IEEE TENSYMP, ICIT, VDAT, IEEE TechSym etc. He is presently serving as the Vice Chair in the Executive Committee of the IEEE Computer Society Technical Committee on VLSI, Editor, IEEE Ethics and Policy in Technology eNewsletters (IEEE Internet Initiative newsletter and IEEE Future Directions newsletter), Associate Editor, IEEE Consumer Electronics Magazine, Associate Editor, VLSI Circuits and Systems Letter, Guest Editor, ELSEVIER Integration, The VLSI Journal. Dr. Ghosal is actively involved in activities of several professional bodies as Senior Member, ACM, Member, IEEE, CSTA, ACM, IAENG, CSI, ISCA, EN etc.

Prof. Dr.-Ing. habil. Michael Hübner is the Chair for Embedded Systems for Information Technology (ESIT) at the Ruhr-University of Bochum (RUB) since April 2012. He received his diploma degree in electrical engineering and information technology in 2003 and his PhD degree in 2007 from the University of Karlsruhe (TH). Prof. Hübner did his habilitation in 2011 at the Karlsruhe Institute of Technology (KIT) in the domain of reconfigurable computing systems. His research interests are in reconfigurable computing and particularly new technologies for adaptive FPGA run-time reconfiguration and on-chip network structures with application in automotive systems, incl. the integration into high-level design and programming environments.

Hai (Helen) Li is currently an Associate Professor in the Department of Electrical and Computer Engineering, University of Pittsburgh, Pittsburgh, PA. Prior to it, she was with Qualcomm Inc., Intel Corp., Seagate Technology, and Polytechnic Institute of New York University. Her research interests include memory design and architecture, neuromorphic architecture for brain-inspired computing systems, architecture/circuit/device cross-layer optimization for low power and high performance. Dr. Hai (Helen) Li is an Associate Editor of IEEE Transactions on Computer Aided Design (TCAD), IEEE Transactions on Multi-Scale Computing Systems (TMSCS), ACM Transactions on Design Automation of Electronic Systems (TODAES), IEEE Transactions on Very Large Scale Integration (TVLSI) Systems, and IET Cyber-Physical Systems: Theory & Applications (IET-CPS). She was the Guest Editor for TCAD, TNANO, TMSCS, and JETCAS. She served on IEEE Computer Society Technical Committee on VLSI (TCVLSI). She was the General Chair of ISVLSI, ISQED and GLSVLSI, and the Technical Program Chair of iNIS, GLSVLSI, ACM SIGDA summer school (DASS), and ACM/SIGDA Outstanding PhD Dissertation Award. She also served on the Executive Committee of ISVLSI, GLSVLSI and iNIS, and the Technical Program Committee of DAC, ICCAD, DATE, ASPDAC, ISVLSI, etc. She received the NSF Faculty Early Career Development Award (CAREER) in 2012, DARPA Young Faculty Award (YFA) in 2013, the Best Paper Award from ASPDAC in 2015, the Best Paper Award from ISVLSI in 2014, the Best Paper Award from GLSVLSI in 2013, the Best Paper Award from ISQED in 2008. In addition to these awards, she also received six Best Paper Nominations from DAC, ICCAD, ISLPED, ASPDAC, DATE, and ISQED.

Dr. Anirban Sengupta is currently an Assistant Professor in Discipline of Computer Science and Engineering at Indian Institute of Technology (I.I.T) Indore, where he directs the research lab on ‘Behavioral Synthesis of Digital IP core ’. He holds a Ph.D. & M.A.Sc. in Electrical & Computer Engineering from Ryerson University, Toronto (Canada) and is a registered Professional Engineer of Ontario (P.Eng.). In the past, he was also affiliated with Indian Institute of Science (IISc) Bangalore as a visiting research scholar. He holds an external affiliation as ‘Honorary Chief Scientist’ at VividSparks IT Solutions Pvt Ltd. His research interest includes Hardware Accelerators, High Level Synthesis, Fault Secured High Level Synthesis, Trojan Security Aware HLS, Hardware Trust in High Level Synthesis, IP core Protection during HLS. His research/sponsored projects are funded by Department of Science & Technology (Science &
Jun Tao is currently an Associate Professor in the Department of Microelectronics, Fudan University, Shanghai, China. She was a Visiting Scholar with the Department of Electrical and Computer Engineering, Carnegie Mellon University, Pittsburgh, PA, USA, in 2012. She received the B.S. and Ph.D. degrees in Microelectronics from Fudan University in 2002 and 2007 respectively. Her research interests include Electronic Design Automation and bio-chip design. Her research/sponsored projects are funded by National Natural Science Foundation of China (NSFC), the National Major Science and Technology Special Project of China, etc. Dr. Jun Tao served on the Technical Program Committees of International Workshop on Timing Issues (TAU) 2011, IEEE International Conference on Computer Design (ICCD) 2012 and ICCAD workshop of Design Automation for Analog and Mixed-Signal Circuits 2012.

Dr. Mike Borowczak is currently a Professor of Practice in the Computer Science department at the University of Wyoming, where he leads the Cyber, Education and Research Center (CEDAR). He earned his Ph.D. in Computer Science and Engineering (2013) as well as his BS in Computer Engineering (2007) from the University of Cincinnati. His research focused on detection and prevention of information leakage from hardware side channels. Mike's current research interests include developing homomorphic encryption, compression and parallelized algorithms for streaming and pseudo-streaming data sources while developing authentic cyber learning experiences. He is also an executive committee member of the IEEE Computer Society, and as a National Science Foundation GK-12 Fellow - teaching and bringing real-world STEM applications in two urban high schools. Since then, he has worked with industry on projects. Mike has authored peer-reviewed articles and papers, presented at national and international conferences, and taught undergraduate/graduate courses in Computer Security, Data Mining, VLSI and Pedagogy in STEM. Mike is an active member of the IEEE, ASEE, ASTE, among others.
Dr. Saket Srivastava is a Senior Lecturer and Program Leader (Electrical Engineering) in School of Engineering at University of Lincoln, UK. He earned his B.E. in Electrical and Electronics Engineering from the National Institute of Technology, Tiruchirappalli, India (2003) and Ph.D. in Electrical Engineering from the University of South Florida, Tampa (2008). He was a postdoctoral research fellow in the School of Electronics and Computer Science, University of Southampton, UK (2008-2010) and an Assistant Professor at the Indraprastha Institute of Information Technology, Delhi, India (2010-2013). He joined School of Engineering at University of Lincoln in 2013. His research interests include probabilistic modeling of emerging nanoelectronic devices, reconfigurable hardware design, embedded systems and software-defined radios. Dr. Srivastava has served on the Technical Program Committee for a number of conferences in Circuits and Systems (DATE, GLSVLSI, ISCAS, VLSI, iNIS) and is a reviewer for several top-tier journals (ACM-JETC, TNANO, TCOMP, TVLSI, IET-CDT). Dr. Srivastava currently serves on the technical program committee of many IEEE meetings including IEEE Computer Society Annual Symposium on VLSI and IEEE International Symposium on Nanoelectronic and Information Systems.