The Story behind the Intel Atom Processor Success

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Editor’s note:
Many state-of-the-art designs, besides their technical challenges, require robust project execution to meet their target. This article presents the Intel Atom processor as an example to analyze—from its management perspective—the effectiveness of project execution, including organizational structure and geographical distribution, timely decision making, milestone definition, tracking progress, and fast recovery from surprises.
—Yervant Zorian, Virage Logic

The Intel Atom processor, a radically new design that makes possible a wide range of new mobile products, is Intel’s smallest processor, built with the world’s smallest transistors, and manufactured on Intel’s industry-leading 45-nm high-k metal gate technology. Silverthorne, the code name for the first processor under this brand, features a $10 \times$ reduction in power consumption. The project assumed large risks, yet it delivered highly functional silicon well ahead of schedule.

The Intel Atom processor (see Figure 1) was specifically built for netbooks and nettops, enabling the design of easy-to-use mobile devices with plenty of performance for a productive and user-friendly online experience. These devices provide a highly mobile option for education, photo and video viewing, social networking, voice over IP, e-mail, messaging, browsing, and several other Internet activities and basic applications. The Intel Atom processor also enables the freedom and flexibility of pocketable Mobile Internet Devices (MIDs), letting users enjoy entertainment or access to the full Internet while on the go.

Its small size and performance per watt enable the Intel Atom processor to provide a range of features, including

- a thermal-power envelope from below 1 W to 3 W, based on industry-leading benchmarks (EEMBC) and leading Web-page-rendering performance;
- greater energy efficiency for mobile devices enabled by low average power and idle power, while scaling performance from 800 MHz to 2 GHz;
- power-optimized front-side bus of up to 533 MHz for faster data transfer on demanding mobile applications;
- multithreading support;
- improved performance on multimedia and gaming applications with support for Streaming SIMD Extensions 3 (SSE3: extensions to the original IA32 architecture);
- improved power management with new Deep Power Down (C6)—a mode the processor can be put in when idle to dramatically lower power dissipation—enabled on the Intel Atom processor Z5xx series for MIDs, and extended C4 states enabled on the Intel Atom processor N270 for netbooks, in addition to non-grid clock distribution, clock gating, CMOS bus mode, and other power-saving architectural features; and
- high performance to run the full Internet and a wide range of other software applications.

Project execution
Intel’s Mobility Group vice president, Elenora Yoeli, led the design engineering for this processor. Yoeli managed this effort with a team located at Intel’s facility in Austin, Texas. The first processor in the Atom project development was code-named Silverthorne. The initial charter of the Silverthorne project was to provide a $10 \times$ reduction in power (relative to previous processor generations) while retaining instruction set compatibility, specifically with the Intel Core2 Duo instruction set architecture. It was further constrained with an aggressive execution schedule (significantly shorter than for previous comparable designs), a reality that ran counter to the magnitude of the technical task at hand. Yet, ultimately,
Silverthorne completed early while meeting the project’s technical requirements.

Looking back at this success, Yoeli specified six areas of focus that had a significant, positive impact on Silverthorne’s execution:

- a carefully crafted microarchitecture;
- a small, experienced project team, colocated and with a flat organization;
- timely decision making;
- aggressive but achievable project goals and the means to trend progress (that is, to predict if Intel was on track for schedule or design targets long before reaching them, which permitted Intel to take early corrective action if needed);
- clear, high-quality milestone definitions; and
- fast recovery from surprises.

Carefully crafted microarchitecture

Early in the project, it was decided that Silverthorne would have to be a new microarchitecture to achieve the desired dramatic reduction in power. Although risky, the decision to proceed with a new microarchitecture also helped establish a mindset in the team from the beginning that achieving power targets were hugely important and that dramatic actions would be necessary to meet them. It also set a clean slate going forward that allowed all new features and changes to be evaluated on the basis of power. Only the most power-efficient features were added, and smart algorithms were employed to improve efficiency with an eye toward optimizing performance per watt. A rough rule-of-thumb trade-off applied across the project was that any feature or change incorporated in the design needed to provide 1% performance for 1% or less power (see Figure 2). Design ideas that required a 2-to-3% power increase to achieve just 1% of performance were generally discarded.

In addition to creating a from-scratch microarchitecture design and pursuing a power-centric decision process, the Silverthorne project team built the processor on Intel’s leading-edge 45-nm process technology. This technology uses dramatic new materials, including hafnium-based circuitry and Intel’s 45-nm high-k metal-gate silicon technology, to reduce processor energy consumption at the device level. Hafnium is a silver-gray chemical element that is highly ductile, corrosion resistant, and chemically most similar to zirconium. Intel engineers discovered that introducing hafnium into silicon chips helps reduce electrical leakage, thereby enabling smaller, more energy-efficient and performance-packed processors.

From the inception of the Silverthorne project, there was little ambiguity on the importance of power or on the project priorities that would drive decision making. Major early decisions (the new microarchitecture and the 45-nm process) let the design team know, unmistakably, that the goals were clear and that the management team was willing to take the risks necessary to create a truly breakthrough product.

Experienced and colocated project team

As with the decisions on designing a new microarchitecture, there were also early decisions made...
regarding both the team and design data organization that were focused on keeping communication and coordination clear. An overriding theme in the project organization was to keep it lean and simple.

The team that designed Silverthorne was small (much smaller than previous teams that had done an IA32 processor design from scratch) but experienced, and it was located at one site. A significant majority of the team had worked together previously on other CPU projects. The team was organized with only a minimal management hierarchy (a project manager, a staff of team leaders, and individual contributors). This flat organization maximized communication across all levels of the project. The staff members typically managed some vertical team that was delivering one portion of the chip (for example, the memory subsystem or the execution units). These same staff members also covered various horizontal functions that coordinated certain activities across the entire chip—for example, RTL delivery or certain design methodology flows. By having staff members “wear two hats,” the multifunctional approach kept the staff population lean but also kept the leads better in touch with the details. The small Silverthorne staff team had a clear view of the project that ran both wide and deep. In general, the team was much flatter (fewer managers) and the “two hats” was a new approach.

While this organization was designed to allow efficient execution against clear goals, it also provided a nimble team with a “can do” mind-set. Problems tended to be found early and once found the team could quickly address them without a lot of bureaucracy. There was also an interesting side effect of the small team size: difficult problems could not be solved by “throwing bodies at the problem.” Instead, the team’s small size helped to force solutions that were necessarily simple and elegant, and more often than not these solutions were also desirable in terms of reducing functional validation risk and staying in line with power targets.

Finally, the team’s size and nimbleness drove and used an efficient design methodology. The team implementing and supporting design automation was part of the overall Silverthorne team in Austin, and the members of this design automation team participated in the design from the beginning. In fact, they were as highly vested in Silverthorne’s success as any other designers and were a key part of project problem solving. The fundamental approach to the chip’s physical design was, like the project organization, relatively flat and simple. The design had only two levels: the full chip and the functional blocks. This allowed full-chip builds and analysis to be turned very quickly. The functional blocks themselves minimized custom design as much as possible, relying heavily on cell-based designs. When custom blocks were absolutely required, they were designed to provide all the design collateral required by a cell-based design approach. As a result, concurrent design was possible even on complex analog design functions.

Timely decision making
As already discussed, there were examples of key early decisions that set the tone and direction for the project before full execution even started. It was essential to have decision making that was both informed and timely to set the project on the right course initially, but such decision making was required throughout, for the project to continue successfully.

Decisions within the project were made by clearly designated “owners,” and ratified as needed by the project manager. Given the flat organization and the horizontal and vertical nature of the team leaders, these decisions typically were made quickly. In general, senior technical experts drove decisions, using relevant data. Valuable resources (engineers, time, and computing resources for simulations) were used during the full duration of project execution to provide the data needed for ongoing decisions.

Decisions (for example, potential changes to features, frequency, power, or schedule) that would impact other Intel organizations outside the project were made in clear and well-established forums with the relevant stakeholders from senior management, manufacturing, marketing, packaging, and so on. Yet, even decisions with broad impact were made quickly and did not negatively affect or impact execution.

Aggressive but achievable project goals
Very early in the project, the Silverthorne team set project goals and schedule milestones that were notably aggressive yet credible and achievable. There was significant emphasis on completing critical milestones early—for example, an initial major goal was to complete all RTL coding in one year. There was also considerable emphasis on reducing execution risk by trailblazing new methods, tools, and design automation flows as early as possible. The senior
staff agreed on these goals, and the entire team understood them from the beginning.

An enhanced theory-of-constraints model was used by the project team to identify and manage schedule-critical paths. With this model, the team evaluated the project milestones on a best-case schedule basis, built a network of dependencies that drove each milestone, and then held in reserve a schedule buffer that was spent only if necessary to respond to specific surprises. The model’s implementation was at a level of detail such that every person on the project could see precisely how his or her work affected critical paths. This model not only provided visibility to the management team but also identified areas of accountability from the entire team. Each week, it was clear to the entire team where things were in terms of actual project schedule versus plan (see Figure 3).

What was even more important was that the model provided trend information that allowed early indication if the end date was in trouble; early indication allowed early action to correct the course. Many Intel projects use this model now, but in the past, most schedules were devised with a built-in buffer for every milestone rather than have a generic buffer built in at the end. The new model is superior because it accommodates those portions of the schedule, which cannot be predicted, that turn out to be more difficult than originally planned for.

The schedule model also provided very detailed analysis of the top schedule-critical paths. Project execution meetings were often structured around detailed analysis of these paths so that the team could take immediate and effective corrective action. Reviewing and solving details of potential problems in the paths helped the management team stay connected to feedback they received from lower-level team members. People working on the critical path were often put in a “protected zone,” where they could be exempt from any meetings or distractions not directly associated with

Figure 3. Project-level Silverthorne schedule report. (SLT: Silverthorne; BNL: Bonnell; POR: Plan Of Record. Bonnell is an internal code name for another version of Silverthorne that was being designed in parallel.) In 2005 there were 53 work weeks on the internal calendar since WW01 covered only 1 January.
addressing issues in the path. The project organization structure and decision-making processes enabled quick and nimble strategic realignment of resources as needed to attack critical paths.

In addition to the project schedule status just discussed, the project status on technical issues (for example, timing convergence or RTL validation) was managed with frequent review of actual data and technical indicators (for example, the number of validation test cases passing for certain scenarios, or the number or circuits in a block which were not yet tuned to run at the target frequency). As with schedule data, it was important that the technical indicators conveyed more than current project status; they also indicated the rate of design progress so that threats to upcoming milestones could be predicted and attacked early. There was very little “management by PowerPoint.” Instead, project managers relied almost completely on the technical data issuing out of the design tools and schedule feedback coming from the theory-of-constraints model.

Clear, high-quality milestone definition

The Silverthorne project team had a clear “do it once” mind-set that affected milestone definition. This made milestones more difficult to hit but greatly reduced the overall project risk resulting from rework, or “invasive late edits.” Specific examples include the following:

- There was a focus on frequent detailed power estimates and simulations from the beginning of the project, performed regularly with each update of the project design data. This allowed the designers to always know how close they were to the power goals and to make incremental design changes along the way to hit those goals without major redesign. A similar approach was used for other processor attributes, such as clock frequency and chip area; the early focus on power for Silverthorne was new and consistent with the project focus on power.

- Clear expectations were identified at the outset so that the team would meet all milestones and deliverables completely and avoid rework. For example, DFT features were fully designed and coded early enough to obviate the need for any rework to add them.

- Design for debug (DFD) features were managed as part of the mainstream processor design execution, subject to the same power, area, and schedule constraints as other functions.

Clear milestones meant that the schedule feedback provided by the theory-of-constraints model had more credibility because the milestones themselves were complete. Milestones did not exclude or underestimate the scope involved in areas of work that have historically caused late schedule excitement on some projects (for example, late DFT functionality or having RTL coding that is functional yet does not meet timing requirements).

Fast recovery from surprises

The team organization and mind-set were cultivated to encourage the frequent flow of accurate data and communication across the project’s disciplinary areas. One desired benefit of this, communicated frequently from the management team, was the ability to find “bad news” early. Although it is always a goal to have no surprises, it is wise to be prepared for them. They do happen, and they tend to happen at very inconvenient times. There was a certain amount of what could be called paranoia on this from the Silverthorne team, made even more acute by the risks associated with a new microarchitecture and a new manufacturing process.

The paranoia was wise, however, because surprises did hit Silverthorne during execution. There were late design discoveries, some coming as the inevitable side effects of working on a lead process—meaning no products had yet been released on that process. But when such discoveries did occur, the project’s organization and decision-making process made recovery quick, though not necessarily painless. Pushing to find bad news early and then being prepared to refocus the team to act on it immediately, allowed the Silverthorne team to work through some major surprises without suffering setbacks to the schedule.

The first Silverthorne silicon was several months ahead of initial schedule. It booted Linux, Windows XP, and Windows Vista (without turning off any design features to successfully boot) within 14 hours of being in the lab in Austin, Texas. Subsequent progress and silicon health—being close to the design targets of functionality, frequency, and power—allowed the program to move quickly forward, with Silverthorne launching as planned in Spring 2008 as the Intel Atom Processor. The principles described here continue to be applied for all new designs in the Intel Atom Processor family of products.
Acknowledgments

This article is based on a presentation originally created and presented by Elenora Yoeli at the 45th Design Automation Conference Management Day. Yoeli is vice president and director of Low Power Intel Architecture (LPIA) Microprocessor Development for the Ultra Mobility Group at Intel. She is responsible for development and post-silicon engineering of low-power, highly integrated microprocessor products for mobile Internet devices. She is also responsible for development and post-silicon engineering of microprocessors for low-cost Intel architectures and SoC products used in consumer electronics. Yoeli oversees design teams located in Austin, Texas; Chandler, Arizona; and Penang, Malaysia.

Bibliography


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