The purpose of this presentation is to describe IC hardware testing – design-for-test, test methods and production testing practices.

Briefly … we will also describe some emerging methods that are changing IC testing.
Outline

• Purpose of testing – failure types & flows
• Automatic Test Equipment (ATE, Testers)
• List of typical Tests
• Functional vs. structural testing
• Design-for-Test
  • Scan design, Memory BIST, Logic BIST
  • On-chip clock generation
• Reliability Defect Screening
• Test Challenges/Opportunities
  • End-to-End Optimization (data consolidation)
  • Adaptive Test, Statistical Test, Outliers
  • Testing of 3D, 2.5D & multi-chip packages
  • Fault Tolerant Designs/Architectures
Integrated Circuit (IC) Test Steps

Inline Test → Wafer Test → Package-level ‘Final Test’ → Board, System Test

Test each die on all wafers
For this presentation, I’ll mainly discuss “Wafer” and “Final Test”.

Test each die on all wafers.

- Inline Test
- Wafer Test
- Package-level ‘Final Test’
- Board, System Test
Wafer-level Testing

1. **Probe & test every die**
2. **Create “Wafer Map” -- showing passing / failing die**
3. **Diamond saw cuts between all chips**
4. “**Passing die**” are selected – put in bare die banks.
5. **Place bare die on package.**
Package Types

Single chip packages

Multi-chip packages

MCM

3DIC
Purpose of Test

- The primary purpose of testing is to ensure the shipped IC will function correctly in the client’s application.
  - Ensure IC is defect-free
  - Ensure IC will function at required performance and at power specifications
  - Includes device repair (mainly RAM redundancy … also spares/partial goods for some ICs)
  - Some designs require power/performance personalization (e.g., Dynamic Frequency Voltage Scaling chosen by on-chip fusing)
  - Reliability ‘aging’ … burn-in
Miles of Wire, Billions of Connections
Defects / Faults

- Historically, production testing has mainly focused on defecting “spot defects”.

- Additional material / shorts

- Missing via

- Gate oxide short

- Bad implant

- Missing metal/open
Another chip layout example

Testing … ensure fabricated die is defect free.

A key trend is that there are more & more failures due to “systematic defects – driven by difficulty of fabricating IC layouts”
Purpose of Test (con’t)

• Also, testing helps to enable design & fab/process learning through characterization testing & data collection.

  • Failure data collection – enabling defect characterization and localization. (e.g., memory bitmapping, logic fail data)

  • Parametric IC characterization – e.g., timing/FMAX measurements, power/IDDQ, …

  • Process monitor data – e.g., on-chip ring oscillators
Automatic Test Equipment (ATE) Types

Typical ATE costs $500K -- $2M

ATE vendors: Teradyne, Advantest, LTX-Credence

Burn-in oven
Example Test Flow

Wafer Test (Ambient)
- Basic functionality check
- RAM test & repair
- Reliability voltage stress
- Process Monitor measurements

Package-level Test (HOT)
- Full coverage tests (99%)
- Delay/performance Tests
- RAM test & repair
- IO parametric testing

Some products do “hot wafer test” ... and “cold final package test.”
Some products only test at one temperature.
Example Test Flow with Burn-in

**Wafer Test (HOT)**
- Basic functionality check
- RAM test & repair
- Reliability voltage stress
- Ring oscillator measurements

**Package-level Test (Cold/ambient)**
- Quick functionality check
- RAM test & repair

**BURN-IN**
- High voltage (1.3X)
- High temp (120C)
- Exercise logic & RAMs

**Package-level Test (HOT)**
- Quick functionality check
- RAM test & repair

**Package-level Test (Ambient)**
- Full coverage tests (99%)
- Delay/performance Tests
- RAM test & repair
- IO parametric testing
Types of Tests

- **Patterns**: ... 0s/1s in & out of the chip
  - Logic & embedded memories
  - Applied at different “corners”
    - VDD – e.g., high, low, nominal
    - Speed – slow / fast
    - ‘Special’ corners – e.g., “VDD bumps”
  - Includes RAM “repair” – replace defective cells with spares
    - Redundancy in logic is also becoming more common

- **Parametric tests**: measure voltage, current, speed

- **Core-specific tests**: High-speed serial IOs, PLLs, TVsense, ...

- **Reliability screens**: Articially age chips ... try to break weak chips (e.g., burn-in)
List of Typical Tests

- IO contact tests (open / shorts)
- Chip leakage (IDDQ)
- Logic testing (0s/1s) -- scan, functional
  - Slow (stuck-at), fast/delay
- Process Monitor structures (Ring Oscillators, etc)
- Electronic chip ID (ECID) tests
- Memory tests (mostly built-in self-test / BIST)
- IO parametric testing
- High-speed serial (HSS) IO testing
- PLL tests
- Analog core tests
- ‘Partial good’ tests (for selected ICs)
- High-voltage stress tests (reliability)
From 90nm -> 32nm, “single threshold" IDDQ testing loses significant test effectiveness for finding single defects.

IDDQ is predominantly used today as a leakage process monitor.
Test Background – Functional vs. Structural Testing

**Functional Testing**

- **A data**
- **B data**

---

**Structural Testing**

- **A**
- **B**
- **C**
- **D**
- **E**
- **F**
- **G**

---

- **ALU**
- **Operation select**
- **Output data**
- **OUT**
Test Background – Functional vs. Structural Testing

**Functional Testing**

- A data
- B data
- Traffic
- Trash
- Boot Op Sys

**Structural Testing**

- Scan Tests
- Logic BIST (LBIST)
- JTAG
Functional vs. Structural Testing

- ICs today are predominantly structural tested. (automatic test generation, DFT, …)

- If structural testing achieves very high fault coverage – why is functional testing required?
  - *Power / performance correlation to system is better.*
  - *Close coverage ‘holes’* (often easier to port from system back to ATE testing)
  - *Early functional verification is done using functional patterns – so tests are available.*

- BUT … full functional testing will dramatically increase the cost of testers & test hardware … and may not be manufacturable.
Design-for-Test (DFT)

- DFT is used extensively on all modern logic ICs (processors, ASICs).
- DFT dramatically reduces test cost, shortens test time, reduces tester cost, improves diagnose-ability and improves test development time/effort.
- DFT Examples:
  - Scan design/LSSD
  - On-chip clock generation
  - IO boundary scan (JTAG)
  - On-chip loopback
  - Test data compression
  - Built-in self test (BIST)
  - Logic BIST, Memory BIST
  - On-chip RAM repair
  - Partial good (multi-core) reconfiguration
SOC Design-for-Test Architecture

- Scan Inputs
- Chip Logic
- RAM
- Register Array
- Scan Chains
- Latches
- Scan Chains
- On-chip clock generation

Test Inputs

CLOCKs

Functional I/O

Scan Outputs
SOC Design-for-Test Architecture

- Scan Inputs
- RAM
- ABIST CNTL
- Chip Logic
- Register Array
- Scan Chains
- Latches
- Functional I/O
- On-chip clock generation
- Scan Chain Inputs
- Scan Chain Inputs
- Scan Outputs
- Chip
IBM Confidential

SOC Design-for-Test Architecture

- On-chip clock generation
- Chip Boundary
- Boundary Scan Latch
- Embedded IP/Cores
- DFT & BIST Circuitry (e.g., SRAMs)
- Functional I/O
- Functional I/O
- Test Inputs
- CLOCKS
- Clock generation
- Test Inputs
- Scan Inputs
- Scan Outputs
- Latches
- Scan Chains
- RAM
- ABIST CNTL

IBM Confidential
SOC Design-for-Test Architecture

On-chip clock generation

Boundary scan DFT circuitry for signal inputs & outputs

Functional I/O

Test Inputs

Functional I/O

Test Inputs

CLOCKS

On-chip clock generation

Latches

Scan Chains

Register Array

Chip Logic

Boundary scan DFT circuitry for signal inputs & outputs

Scan Inputs

Scan Outputs

Boundary Scan Latch

Chip Boundary
On-chip clock generation

High speed clocks generated on the IC. (slow speed signals from testers)
IO Testing – Bi-directional

Tests

1. 0/1 logical/slow
2. Delay tests
3. Driver voltage tests (min 0/1)
4. Receiver voltage tests (min 0/1)
5. IO leakage
Tests
1. On-chip loopback test
Fault Models

• To automatically generate test patterns, the software must have a model representing defect behavior – called a “fault model”.

Stuck-at fault model
Each gate input & output can be permanently stuck at logical ‘0’ or ‘1’
(6 faults for NAND gate below)

Transition fault model
Used for AC/delay test generation.
Each gate input & output can have a slow transition (rising or falling).
Automatic Test Pattern Generation (ATPG)

• Scan design converts the sequential circuits into a combinational one for ATPG by adding a ‘scan port’ to all flip-flops (latches, registers).
  • *ATPG for sequential circuits has been found to be “computationally impossible” for large circuits (e.g., >50K logic gates)*

• Structural Testing – gate-level test of logic circuits by detecting a high number of modeled faults.
  • *Stuck-at fault coverage:* >98%
  • *Transition fault coverage:* >80%

• Patterns are automatically generated
  • 5,000 – 20,000 patterns are typical
Logic Testing

- A difficulty of scan-based logic testing is the large amount of data volume needed. (and test time)
  - \( \text{Scan data volume} = \text{number of test patterns} \times \text{number of scan latches} \) (gigabytes & gigabytes)

- The industry has moved to “test data compression” – encoding test data.

- One method is “OPMISR+” test data compression.
  - There are other methods such as “Test Kompress” and “DFTMax”.

- Logic BIST is a form of test data compression – patterns are generated on-chip and output data is fully compressed.
Logic BIST (LBIST)

On-chip pseudo-random pattern generators (PRPGs) generate input data.
On-chip multi-input shift registers (MISRs) compress output data into a relatively short signature.
• LBIST offers the benefit of virtually no test data volume.

• BUT … LBIST takes more patterns to achieve the equivalent fault coverage.

• Test data compression (OPMISR+) comes close to achieving the ultimate coverage of deterministic test patterns with dramatically less data volume (40X-100X).
Double the number of scan inputs
Fanout out a single scan input to many internal scan chains
Embedded RAM Testing

• RAMs: embedded SRAMs, embedded DRAMs, Embedded TCAMs

• Tested with BIST engine – that creates all 0/1 patterns and compares results with expected. (all done on-chip)
  • *Shared BIST engines – multiple RAMs in parallel*

• Virtually all RAMs today have “extra rows or columns” – redundancy that will replace failing rows or columns.

• BIST engine also enables “memory fail bitmapping” – critical for yield learning
Other Tests

- IO parametric testing
- High-speed serial IO testing
- IDDQ (leakage)
- Ring Oscillator measurements
- Electronic chip ID (ECID) tests
- PLL tests
- Analog core tests
- ‘Partial good’ tests (for selected ICs)
Reliability Defect Screening

• Reliability defects are ones that failures during the life of the IC.
  • The goal is to detect/reject ICs which would later fail in the field to fail at the factory.

• These defects can be accelerated by raising VDD and temperature.

• Burn-in is one method for getting this acceleration.
  • Raise voltage & temperature … and the ICs will “age” by 100X – 1000X the burn-in duration.
  • Burn is relatively expensive … only performed on a minority of shipped ICs.

• A smaller amount of acceleration can be achieved by just raising VDD during production testing.
  • For example, raise VDD during wafer probe testing for a short duration acceleration test.
Fault Diagnosis

• A key role of testing is to collect data for yield learning.
  • Memory bitfail map, logic fail data collection, measurements of parametrics, on-chip process monitors, etc.

• One goal of diagnosis is to identify the circuit or layout feature that caused the chip to fail.

• Fail data is collected from the logic tests.
  • Then off-line software tools are used to identify the failing circuit / layout feature.

• Sometimes “physical failure analysis” will tear apart the chip to understand the defect or process anomaly that caused the chip to fail.
  • Ideally fab feedback will enable this to be fixed.
Emerging Trends
Changing Test Requirements
New Challenges & Opportunities

- On-chip Sensors
- End-to-End Statistical Analysis & Optimization
- Adaptive Testing
- 3DIC & 2.5D IC testing
- Fault Tolerance
Embedded Circuitry for Tuning, Characterization, and Diagnostics

Sensor types

- Voltage monitors
- Temperature
- Noise
- Process monitors (e.g., ring oscillators)
- BIST circuitry (e.g., FMAX, VMIN)
- HSS eye measurements
- Noise injectors
- Clock tuning buffers
- Memory margin tuning
Embedded Circuitry for Tuning, Characterization, and Diagnostics

Emerging chip designs have “hundreds” of these circuits today ... in the near future, there will be “thousands”.

Embedded Circuitry for Tuning, Characterization, and Diagnostics

• This circuitry will also be used in the field – for monitoring, data collection, diagnostics and field adjustment.

Test data from each device at each step will be stored ‘forever’.

This enables statistical analysis of data whenever there are Yield or Quality or Reliability issues.
Historically, there has not been End-to-End analysis across companies.

(unless there is a problem -- then only limited samples/data)
End-to-End Statistical Analysis

- Merge all data collected in the end-to-end test flow.
  - *Electronic ID per device is a key enabler*

- Continual statistical analysis
  - *Identify key correlations*

- Drive down “time to root cause analysis.”
  - *Get to root cause on many more problems*
Ideally, this data is statistically analyzed on a regular basis (nightly?) … and automatically the test recipe is “tuned” to optimize Test, Yield, Quality, Costs, …
End-to-End Data across the Entire Supply Chain

Note that this data will be collected by a number of different companies. Many companies (world-wide) will need to access at least a limited amount of this data.
Adaptive Test

• Today, production Test is (mostly) a series of pre-defined tests applied serially with static conditions and pass/fail limits.

• In future, testing will be constantly changing – where real-time automated analysis is performing continual optimization. (“Adaptive Test”)

• No two chips will ever see identical tests. (with traceability)

• “Everything” will be driven by advanced statistical analysis.
Subgroup to Test & Testability Section of International Technology Roadmap for Semiconductors (ITRS)

www.itrs.net

If you’d like to be added to the distribution list – send email to Phil Nigh  (nigh@us.ibm.com)
Adaptive Test – General View / Test Step

Feedforward data
ChipID-based data, expected yield, historical parametric data & fail bin fallout, capacity & serviceability, inline parametric results, timing/VDD/power conditions

Real-time analysis & optimization (RT A/O)
(yield, failure bins, parametric data)

Test

Post-Test Analysis & Dispositioning (PTAD)
Maverick analysis, statistical bin limits, die segregation, flow changes, data to feed forward to later steps
Adaptive Test Flow

“RT A/O” stands for “Real-Time Analysis & Optimization”

“PTAD” is “Post-Test Analysis & Dispositioning”

Database & Automated Data Analysis
(including post-test statistical analysis, dynamic routings and feedforward data)

- Fab data
- Design data
- Business data
- Customer specs

Assembly Ops.
Includes build operations at any level of assembly

- Fab data
- Design data
- Business data
- Customer specs

Card/System Test

Field Operation
Examples of Adaptive Test

• Perform post-test statistical analysis of data – identify and reject statistical outliers. (test flows could also be changed on per die basis)

• Define parametric limits in real-time by performing “DPAT” – Dynamic Part Average Testing.

• Feedforward data from previous test steps to later test steps to optimize test limits, content and better identify outliers.

• Based on real-time fallout analysis, continuously optimize diagnostic & yield analysis data collection.

• If Maverick or outlier product is identified (e.g., wafer) – perform additional test in real-time to evaluate the Quality/Reliability of ‘passing’ product.

• Perform ‘test sampling’ to optimize test content & limits for remaining product. (e.g., dynamically remove tests that never fail)
Real-time analysis & sampling for Test Pattern Reduction

Test Program
• Pat 1
• Pat 2
• Pat 3
• Pat 4
  • Pat 15000

ASICs
(Final Test)

Off-line analysis – pattern select & sample rate

Regular off-line Analysis plus real-time adaptive pattern sampling has been found to reduce ATPG test time by >50%.
Real-time analysis & sampling for Test Pattern Reduction  

**ASICS**  
(Final Test)

Test Program
- Pat 1
- Pat 2
- Pat 3
- Pat 4
- ...  
- Pat 15000

**High-volume processor**  
(Wafer probe)

Test Program
- Pat 1
- Pat 2
- Pat 3
- Pat 4
- ...  
- Pat 200

Real-time Updates based on sampling

**Off-line analysis – pattern select & sample rate**
“Statistically more Reliable ICs”

Red chips are fails … black & green chips are passes.  

This device … is statistically more reliable than these three devices

Defects cluster
“Statistically more Reliable ICs”

A key goal of Adaptive Test is to perform real-time, automated optimization how “outliers” are manufactured.

- Yield
- Quality
- Reliability
- Delivery schedule
- Supply
- Mfg. Cost
- Customer Satisfaction

This device ... is more reliable than these three devices
3D Packaging

- True “3 dimensional” packaging is coming.
- “3D integration” is fundamentally different from “chip stack technology”.
- Increased bandwidth will dramatically improve performance.

Chip Stack technology
3D Packaging

- True “3 dimensional” packaging is coming. Transistors at each level

- Future ICs will have 10s of 1000s of connections between active layers.

- Power management, Test & yield management are critical issues.

- Do we test at each layer?
- How?
Self-Adjusting, Self-healing, Fault-tolerant Designs

- ICs (and computers) will have much more capability to work around ‘failures’ and ‘aging’.
  - *In-the-field adjust & healing capability*

- Fault tolerant & adjustment circuitry raises interesting test issues.
  - *Use the fault tolerant features for yield improvement?*
  - *Test using adjustment control circuitry ... or remove adjustment circuitry for test.*

- For example, if a design has 100 processor cores ... and only 90 cores are required for functionality ... and system-level testing can determine good/bad cores ... is wafer probe & package test even required? (‘DPM is irrelevant’)
Ideal System

- On-line testing
- Fault-tolerant
- Self-healing
- Graceful degradation
- Redundant systems
- Avoid ‘unrecoverable faults’
- Field adjustable
- Automated diagnostics

[Mark Barber]