

Introduction to the Special Section on Networks-on-Chip

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IT is a great pleasure to introduce the special section on networks-on-chip (NoCs) to the readers of the *IEEE Transactions on Computers*. This special section consists of eight papers that have been selected to cover a wide spectrum of issues in NoC design.

Systems-on-Chip (SoCs) designed at nanoscale will soon contain billions of transistors. This makes it possible to integrate hundreds of IP cores running multiple concurrent processes on a single chip. The design process of such multiprocessor systems-on-chip (MPSoCs) faces a number of important challenges and, consequently, the current design methodology needs to change from computation-based design to communication-based design. This special section focuses on using communication-based design as a new paradigm to design the future MPSoCs.

It is important to note that such a paradigm change requires scalable communication architectures for efficient implementation of future systems. Since neither classical bus-based nor point-to-point architectures can provide scalable solutions and satisfy the tight power and performance requirements of future applications, the NoC approach has recently been proposed as a promising solution. Indeed, in contrast to the traditional solutions, the NoC approach can provide large bandwidth with moderate area overhead. Besides scalability, the NoC approach offers increased reusability and predictability of the design. These features are mainly provided by the use of standard interfaces to connect the IP cores and the structured nature of the global wires. In turn, these well-controlled parameters enable the use of aggressive signaling circuits, which can further reduce the power dissipation and propagation delay significantly.

It is worth mentioning that the focus of this special section is primarily on the large class of application specific NoCs, which have very different requirements compared to the general purpose networks. First, being application specific, most of the design effort goes into optimizing the network for a specific application or class of related applications. Second, as most of these chips are meant to be used in energy constrained environments (e.g., wireless chipsets, cell phones, portable multimedia and gaming devices, etc.), the energy consumption of the network becomes a major design issue. Last but not least, various

implementation and testing issues (e.g., regularity, wiring complexity, clocking strategies, fault tolerance, etc.), as well as security concerns related to the practical utilization of these systems, are also very important. These interesting design trade-offs in designing application specific NoCs have lately generated a huge interest from both academia and industry.

Starting from these overarching ideas, the present special section brings together several outstanding contributions in the area of NoC design. More precisely, these papers make significant contributions while dealing with communication infrastructure and communication paradigm optimization. The first paper of this special section is entitled "Traffic-Balanced Routing Algorithm for Irregular Mesh-Based On-Chip Networks" and is authored by S.-Y. Lin, C.-H. Huang, C.-H. Chao, K.-H. Huang, and A.-Y. Wu. In this paper, the authors describe a methodology for performance optimization in irregular mesh NoCs. This is a significant problem since imposing standard topologies on NoCs can result in poor performance due to the potential mismatch between the communication infrastructure and the application traffic. In terms of technical contribution, the paper presents a lightweight routing algorithm for oversized IP avoidance which improves the classical algorithms for fault-tolerant routing by providing lower latency and higher throughput.

In the second paper, "Adaptive Channel Buffers in On-Chip Interconnection Networks—A Power and Performance Analysis," A.K. Kodi, A. Sarathy, and A. Louri address the issue of low-power design of routers and associated logic for congestion control in NoCs. Indeed, besides performance, power consumption is a major concern in NoC design. By relying on techniques that work at both circuit and architectural levels, the authors propose ways to statically and dynamically allocate the input buffers in routers such that the power consumption is minimized with minimal impact in network performance.

The next paper of this issue is "Concepts and Implementation of Spatial Division Multiplexing for Guaranteed Throughput in Networks-on-Chip," where A. Leroy, D. Milojevic, D. Verkest, F. Robert, and F. Catthoor compare two different approaches for circuit-switched NoCs, namely, time-division multiplexing (TDM) and space-division multiplexing (SDM). Toward this end, the authors propose and evaluate a new SDM architecture (which is implemented as a switched virtual circuit) where an application establishes a virtual channel from source to destination and uses it exclusively. As a result, the authors

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advocate that the use of SDM (rather than TDM) is a better choice for NoCs given the small area and energy overhead.

The issue of efficient clock distribution in future MPSoCs is addressed by F. Vitullo, N.E. L'Insalata, E. Petri, S. Saponara, L. Fanucci, M. Casula, R. Locatelli, and M. Coppola in their paper entitled "Low-Complexity Link Microarchitecture for Mesochronous Communication in Networks-on-Chip." In this paper the authors propose a low-complexity microarchitecture for skew insensitive mesochronous on-chip communication which benefits from low power and small area overhead. The mesochronous design paradigm seems to be particularly suitable for the upcoming deep submicron technologies (a concrete example being given for a 65 nm design) as an effective way to deal with clock skew issues in fully synchronous designs. A distinct advantage of the proposed solution is that it can be easily integrated in the conventional design flow since it relies only on standard cells.

The next two papers included in this special section deal with two complementary concerns of the design process, namely testing and security. Both are important and timely issues that have not received enough attention so far. The first of these two papers, namely, "A High Fault Coverage Approach for the Test of Data, Control and Handshake Interconnects in Mesh Networks-on-Chip," by É. Cota, F.L. Kastensmidt, M. Cassel, M. Hervé, P. Almeida, P. Meirelles, A. Amory, and M. Lubaszewski, addresses the issue of interconnect testing in mesh-based NoCs. In particular, the authors show that the standard approaches in testing cannot be successfully used for NoCs. Instead, they propose an expanded fault model for a basic 2×2 mesh NoC and show how this fault model (i.e., AND and OR-shorts among all pair of wires) works hierarchically for larger NoCs. The next paper, "Secure Memory Accesses on Networks-on-Chip," by L. Fiorin, G. Palermo, S. Lukovic, and C. Silvano, deals with security issues in NoC-based MPSoCs. The main idea is that the advantages offered by the network-based communication architectures may be undermined by new weaknesses that can be exploited during system normal operation. In particular, the authors consider the problem of protecting data from illegal access from unauthorized IP cores and propose a secure network architecture based on data protection units integrated into network interfaces of the NoC. This kind of security-aware design seems to be particularly suited for dynamic systems running multiple applications in a reconfigurable setting.

Finally, the last two papers address two disruptive technologies for on-chip communication, namely, wireless and photonics NoCs. The first paper "SD-MAC: Design and Synthesis of a Hardware-Efficient Collision-Free QoS-Aware MAC Protocol for Wireless Network-on-Chip," by D. Zhao and Y. Wang, advocates for using on-chip wireless radios as a means of replacing traditional wires for better bandwidth utilization, faster communication, and increased flexibility. As such, the authors propose a new wireless NoC architecture which exploits RF nodes placement and clustering and a collision-free synchronous distributed MAC protocol that ensures a certain level of QoS capability. Concrete results from a hardware implementation of a synchronous distributed MAC unit show the

promise of this approach. The second paper, "Photonic Networks-on-Chip for Future Generations of Chip Multiprocessors," by A. Shacham, K. Bergman, and L.P. Carloni, proposes a hybrid NoC architecture that combines a broadband photonic circuit-switched network with an electronic overlay packet-switched control network. The main promise is based on the low loss in optical waveguides that can ensure a much higher bandwidth (and lower latency) at significantly lower levels of power dissipation compared to regular NoCs which are based solely on electronic signaling. The authors consider in detail various design issues (e.g., topology, routing algorithms, deadlock avoidance, etc.) and provide experimental results supporting the feasibility of this approach.

In terms of contents and technical solutions, these papers cover a set of important and timely issues with far reaching implications for future research in NoC design. We sincerely hope that this special section will become a solid reference in years to come. In our view, the authors did a wonderful job in presenting the material and putting their technical contribution in the proper perspective. We would like to use this opportunity to thank them all for this achievement. At the same time, we gratefully acknowledge the effort of all of the reviewers involved in the peer review process; their careful and responsible work, hidden behind the scenes, made the selection of these outstanding contributions possible.

Finally, special thanks are due to the Editor-in-Chief, Dr. Fabrizio Lombardi, for encouraging and hosting this special section and to Ms. Joyce Arnold for excellent support during the submission and peer review process. We hope you enjoy and appreciate the reading.

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Guest Editor



Radu Marculescu received the PhD degree in electrical engineering from the University of Southern California, in 1998. He is currently a professor in the Department of Electrical and Computer Engineering at Carnegie Mellon University, Pittsburgh. Prior to joining Carnegie Mellon University, he was a faculty member at the University of Minnesota, Minneapolis. Dr. Marculescu is a recipient of the US National Science Foundation's CAREER Award (2000) in

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