CALL FOR PAPERS
Emerging Trends and Design Paradigms for Memory Systems and Storage
IEEE Transactions on Emerging Topics in Computing
Special Issue/Section, Second Issue of 2017

The continuing scaling of silicon-based microelectronic technology, as well as the emergence of new, non-silicon-based technologies, enable increasing system complexity and performance, paving the way to applications which had been unthinkable a few years ago. At the same time, an ever-increasing amount of data needs to be stored and accessed quickly, posing new challenges to memory systems and storage elements. IEEE Transaction on Emerging Topics in Computing (TETC) seeks original manuscripts for a Special Issue/Section on Emerging Trends and Design Paradigms for Memory Systems and Storage covering the entire spectrum of relevant research activities, from manufacturing to test, which is scheduled to appear in the second issue of 2017. All aspects of manufacturing, design, test, reliability, resilience and availability of memory systems and storage are of interest, including but not limited to:

1. Emerging Technologies: techniques for resistive, spin-based, phase-change, and bulk-switching memories
2. Yield Analysis/Modeling: defect/fault analysis/models; statistical yield and prediction modeling.
3. Memory Design: bit cells, array/sensing structures, statistical design and margining, interaction of volatile and non-volatile memory
4. Memory System Design: interfaces, compute in/near memory, caching structures
5. Test and Design for Testability: test algorithms; test and variability, interaction of design margins and test, Built-In Self-Test, interfaces, interconnect fabric, NoC, FPGA, SoC, CPU, GPU
6. Error Detection, Correction, and Recovery: self-checking solutions, error-correcting codes, fault masking and avoidance, recovery schemes, redundancy, reconfiguration, resilient design
7. Dependability Analysis and Validation: fault injection techniques, dependability characterization

Submitted articles must not have been previously published or currently submitted for journal publication elsewhere. An extended version of the article appearing in any conference proceedings can be submitted provided that it has substantially new content w.r.t. to the original conference version. The conference paper must be cited in the main text and the cover letter must clearly describe the differences with the conference version and clearly identify the new contributions. As an author, you are responsible for understanding and adhering to our submission guidelines; you can access them at the IEEE Computer Society web site, www.computer.org. Please submit your paper to Manuscript Central at https://mc.manuscriptcentral.com/tetc-CS. Please note the following important dates.

Submission Deadline: June 1, 2016
Reviews Completed: August 15, 2016
Major Revisions Due (if Needed): October 1, 2016
Reviews of Revisions Completed (if Needed): November 1, 2016
Minor Revisions Due (if Needed): December 1, 2016
Notification of Final Acceptance: February 1, 2017
Publication Materials for Final Manuscripts Due: March 1, 2017
Publication date: Second Issue 2017 (June Issue)

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